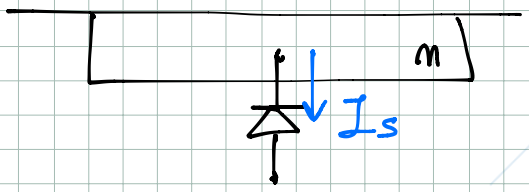
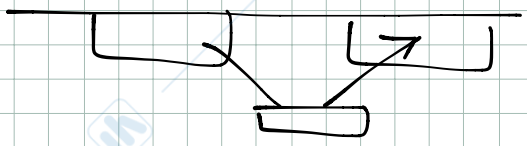
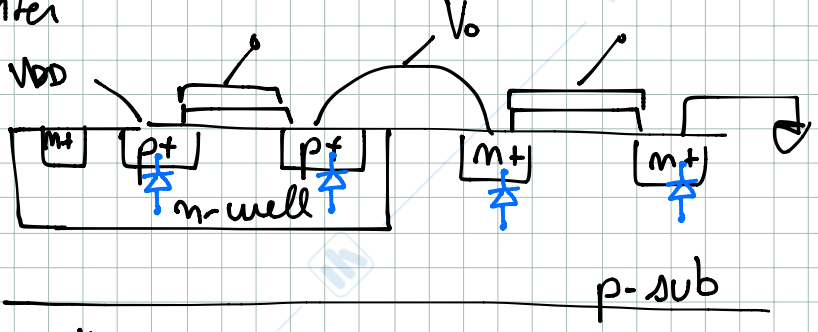
CMOS technology
- leakage
- isolation
- par capacitance

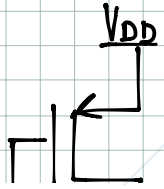
Leakage



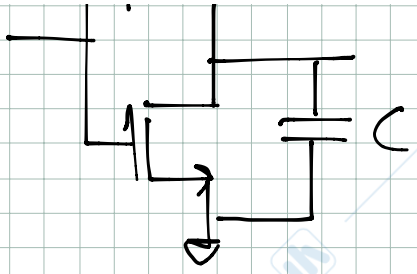


par capacitance inverter





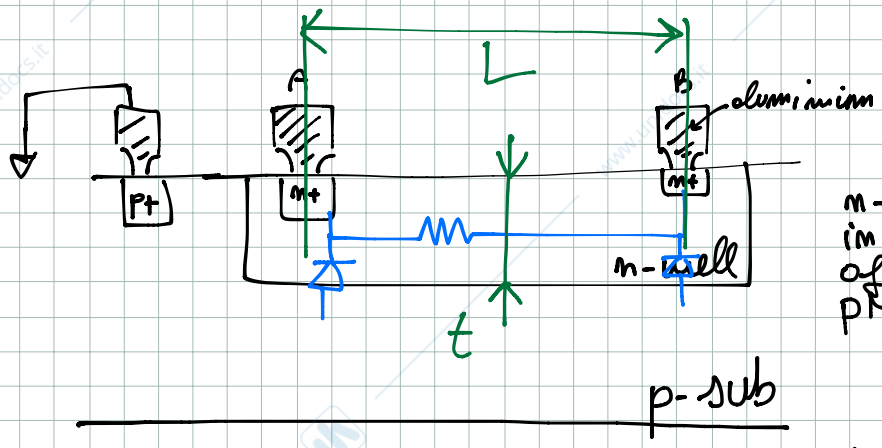
f_{max} depends on C that depends on the contact



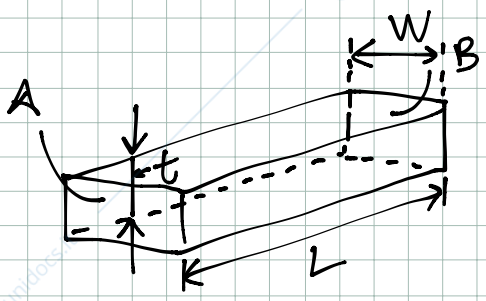
region perimeters that has to be reduced

RESISTORS

Are fabricated in different manners , the simplest way is (psub technology):



n-well is fabricated in the same way of the one for pMOS transistors



$$R_{AB} = \rho \cdot \frac{L}{W \cdot t} = R_S \frac{L}{W}$$

ρ ← resistivity of n-well

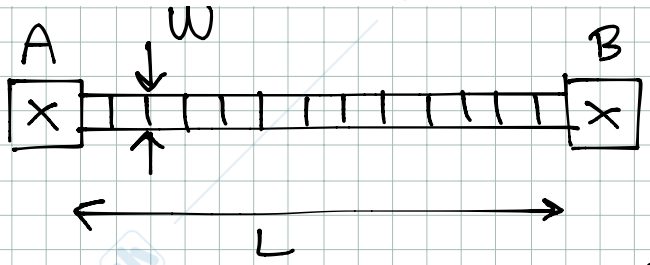
$$R_S = \frac{\rho}{t} \left[\frac{\Omega}{\square}\right]$$

R_S ← SHEET RESISTANCE

Rs

Rs depends on tech process, we can only decide W and L

top view (layout view)



We have to decide the number of squares: $N_\square$

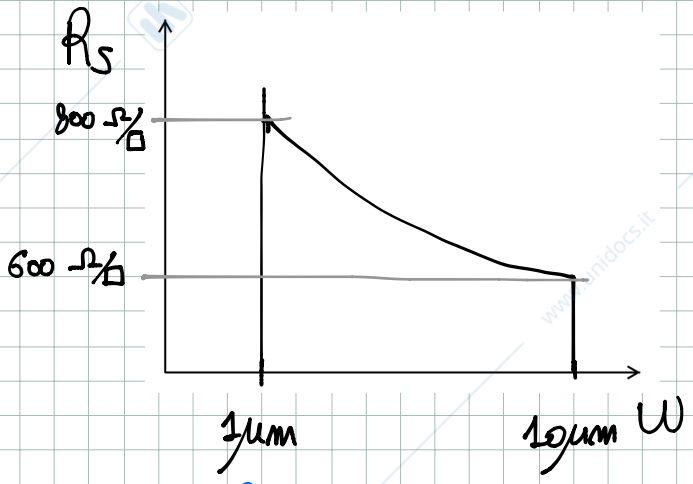
So $[R_S] = \left[\frac{\Omega}{N_\square}\right]$

Ex: if $W = 1\,\mu m$ and $N_\square = 6$

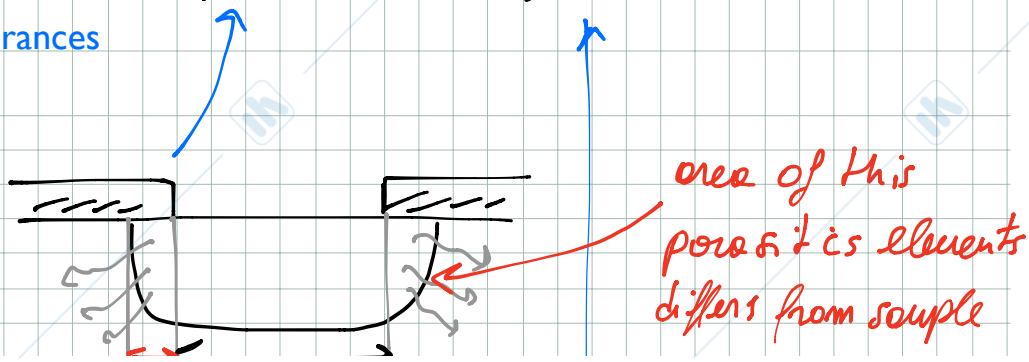
discorso su area res.

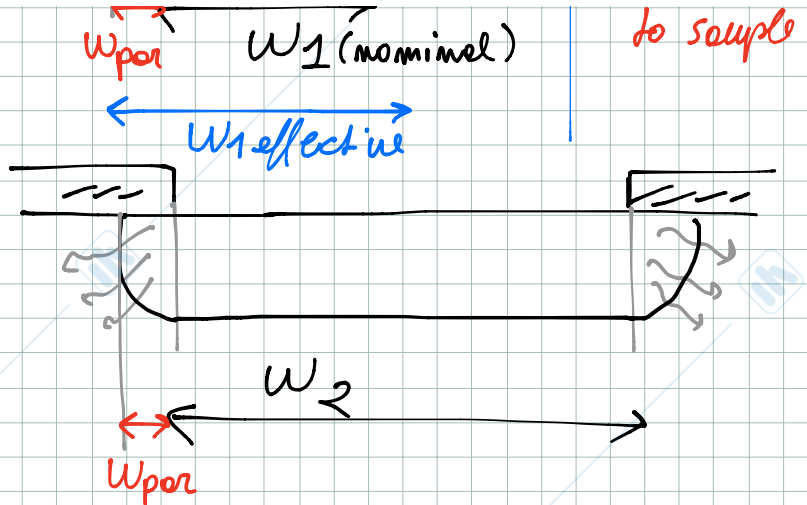
if $W = 3\,\mu m$ and $N_\square = 6$

Quindi R_S = COSTANTE $\cdot \frac{1}{W}$?

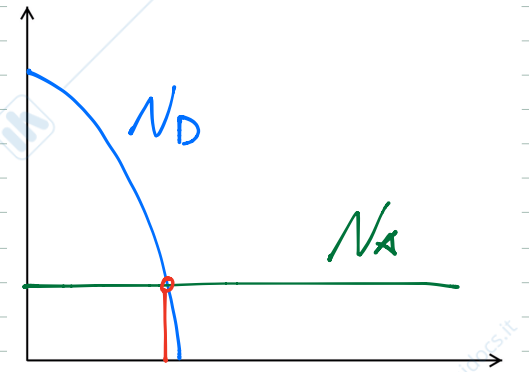


Fabrication tolerances





It's better to use wider resistor because the width of parasitics elements is negligible respect to the considered nominal width, hence, for small W, Rs has a larger uncertainty.



$t \rightarrow$ change for every element

so $t + \Delta t$

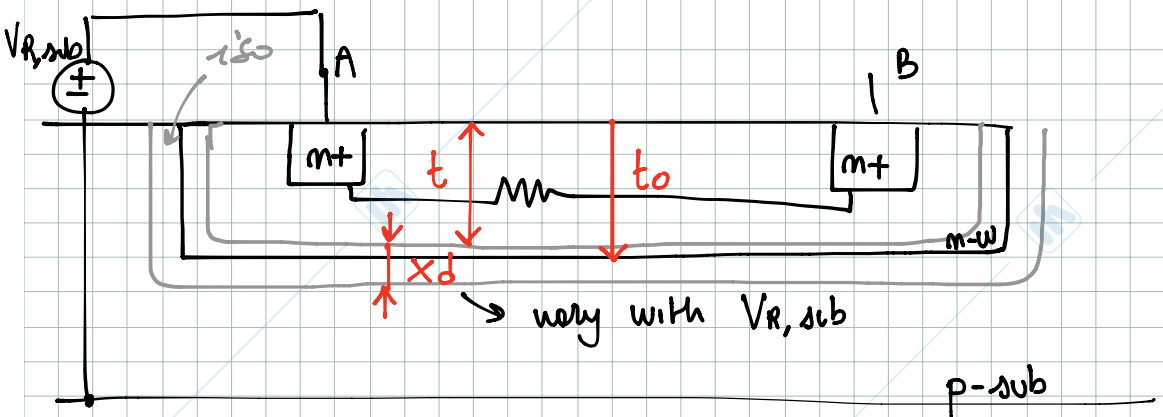
$\rho + \Delta\rho$ $\Rightarrow$ $\frac{\Delta R}{R} \approx 30\%$

Temperature effect

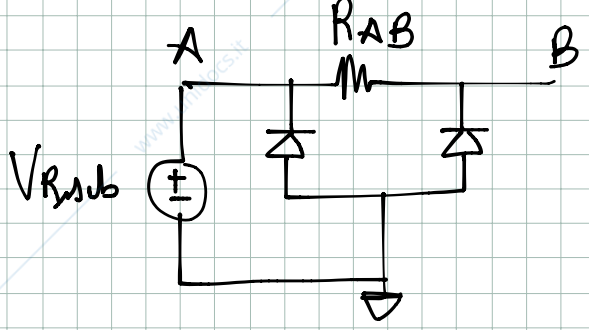
$$R_{AB}(T) = R_0(1 + k_T \Delta T), \quad k_T = 0{,}3\,\%/^\circ C$$

Vr,sub

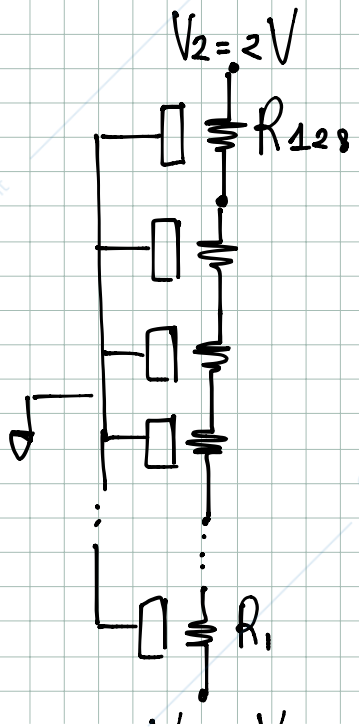
Vr,sub is responsible of resistor tickness variation

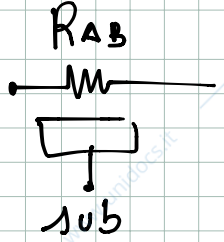


$R_{AB} = f(V_{R,sub})$



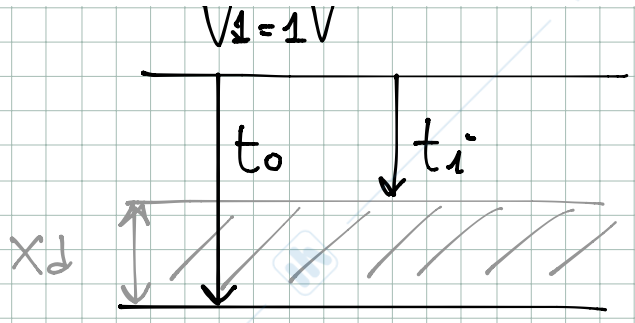
For example, considering a 128 bit DAC with all same values nominal resistances, the variation of Vr,sub for each resistance makes the real values differ from each other





$R_i = \frac{\rho}{t_i} \frac{L_i}{W_i}$

↳ consider only t_i affected by error



t_0 = thickness when $V_{R,sub} = 0$

$t_i = t_0 - x_d$

Considering only ti parameter varying for each resistor we can write:

$$\frac{R_{128}}{R_1} = \frac{\rho \cdot \frac{L_{128}}{W_{128}}}{\frac{\rho}{t_{128}} \cdot \frac{L_1}{W_1}} = \frac{t_1}{t_{128}} = \frac{t_0 - x_{d1}}{t_0 - x_{d128}}$$

$$x_d = \left[\frac{2\varepsilon_0\varepsilon_r}{qN_D}\left(V_{R,sub} + \phi_0\right)\right]^{1/2}$$

$$\Rightarrow \frac{R_{128}}{R_1} \simeq 1 + \frac{1}{t_0}\left(\frac{2\varepsilon_0\varepsilon_r}{qN_D}\cdot\phi_0\right)^{1/2} \cdot \left[\left(1 + \frac{V_2}{\phi_0}\right)^{1/2} - \left(1 + \frac{V_1}{\phi_0}\right)^{1/2}\right]$$

(V_2 = $V_{R,sub}$ 2, V_1 = $V_{R,sub}$ 1)

Ex

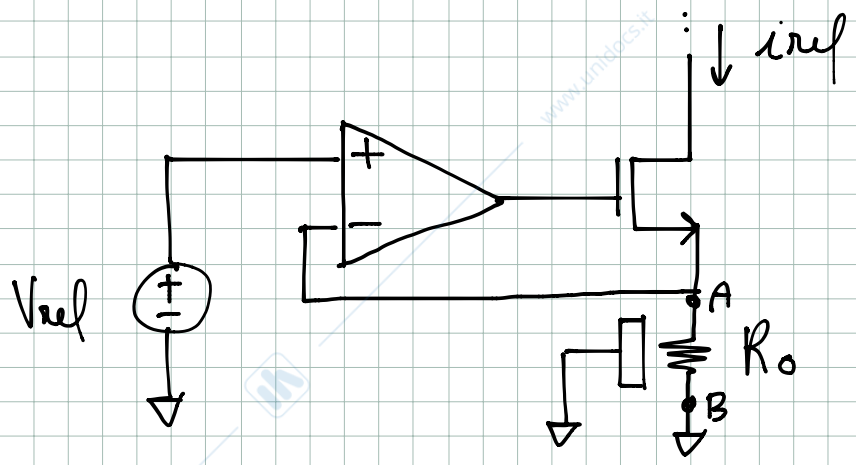
$t_0 = 2\mu m$

$N_D = 10^{16} \cdot cm^{-3}$

$\phi_0 = 0{,}7\ V$ $\Rightarrow$ $\frac{R_1}{R_{12}} \cong 0{,}6$

$V_1 = 1V,\ V_2 = 2V$

Important: Rab=f(Vr,sub) , f is NOT A LINEAR FUNCTION. Is bad because many analog systems are based on reference resistors . For example:



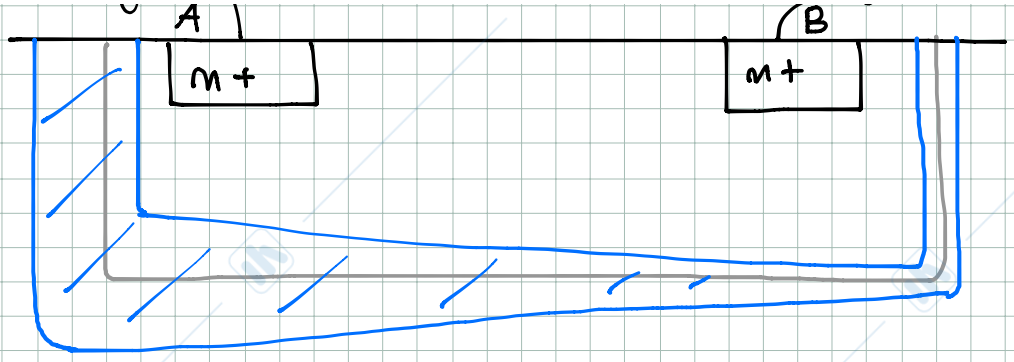
$$iref = \frac{Vref}{Ro(Vr,sub)}$$

V_A and V_B influences Vr,sub

$V_B = 0 \Rightarrow$ ok but $V_A = Vref$

this produces a non homogeneous thickness along the resistor width provoked by a non homogeneous depletion region

Vref



This behaviour can be modeled using two coefficients Be and kv giving us:

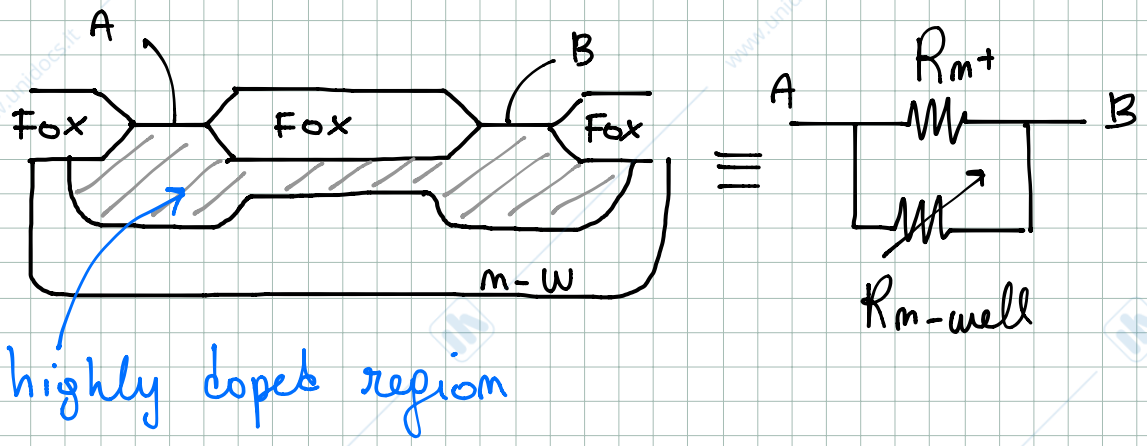
$$R_{AB} = R_0\left[1 + B_e\left(V_{x,sub} - V_{sub}\right) + k_v\left(V_A - V_B\right)\right]$$

for n-well resistors $B_e \cong k_v \cong 10^4 \div 10^5$ ppm/V

we can solve this problem:

1. INCREASING DOPING CONCENTRATION IN THE N REGION since tickness depends on doping level.

For n-diffused resistors it looks like:



The major part of the current flowing into the resistor flows trough the highly

doped region (Rn+) that is not affected by thickness variation, on the other side a negligible part of the total current flows through the Rnwell (instead affected by tickness variation) making the variation of the total Resistance negligible.

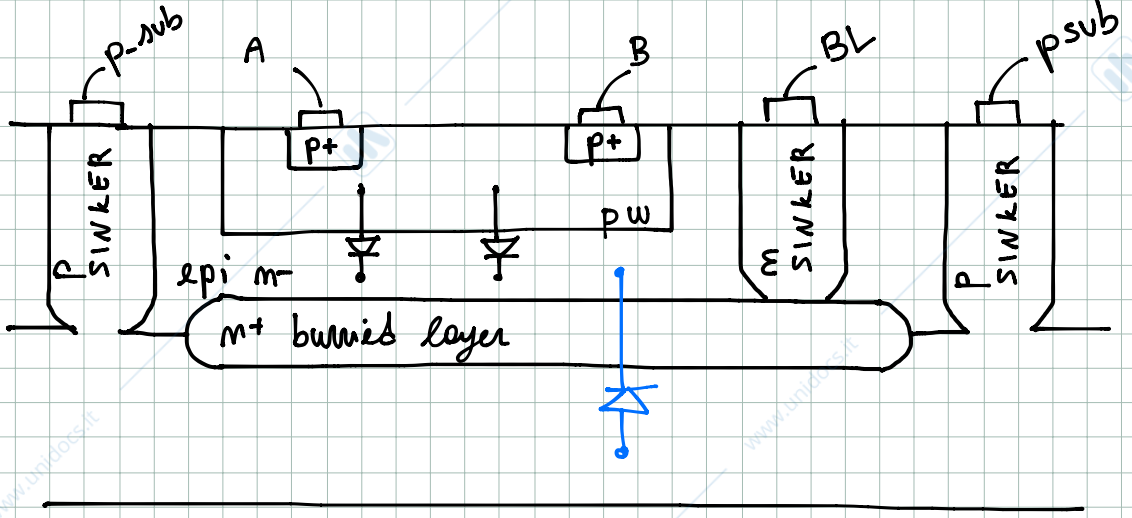
The drawback is that this technique decrease dramatically the value of Rs, so I will need very big resistors!
Typical values are:

$R_S = 2 \div 30 \ \Omega/\square$

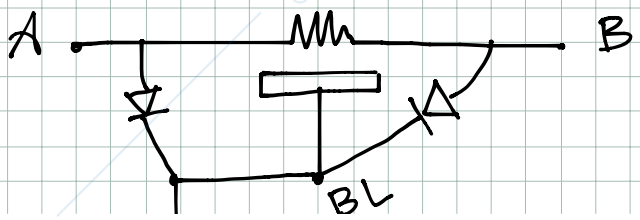
$\frac{\Delta R}{R} = \pm 20\%$, $k_T \cong 10^3$ ppm/°C

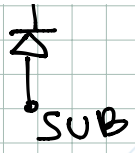
$k_V \cong B_C \cong 10^2 \div 10^3$ ppm/V

2. ISOLATE IN SOME WAY THE RESISTOR

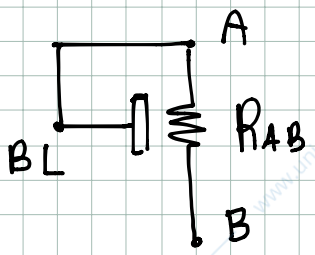


p-sinkers are used to polarize the substrate
The equivalent scheme is:

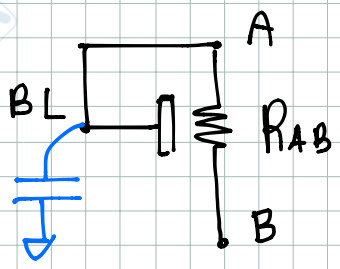




V_{BL} has to be: $V_{BL} > V_A$ or V_B otherwise the resistor will become a short circuit. A solution is to connect BL to A

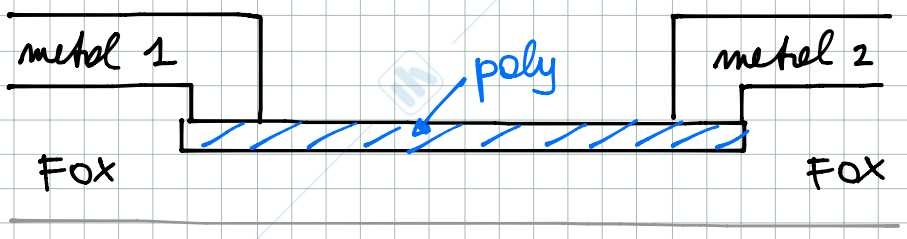


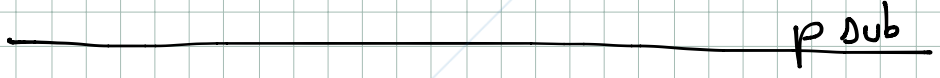
in this way voltages between resistor and substrate does not affect the resistor value.
Drawback: this technique generates a parasitic capacitance from substrate to ground limiting the bandwidth of the circuit in which it's putted.



POLYSILICON RESISTORS

Instead of placing poly layer on the gate oxide it is placed on the field oxide.
Capacitance between R and the sub is small because of FOX





$R_S \hat{=} 20 \div 80\ \Omega/\square$

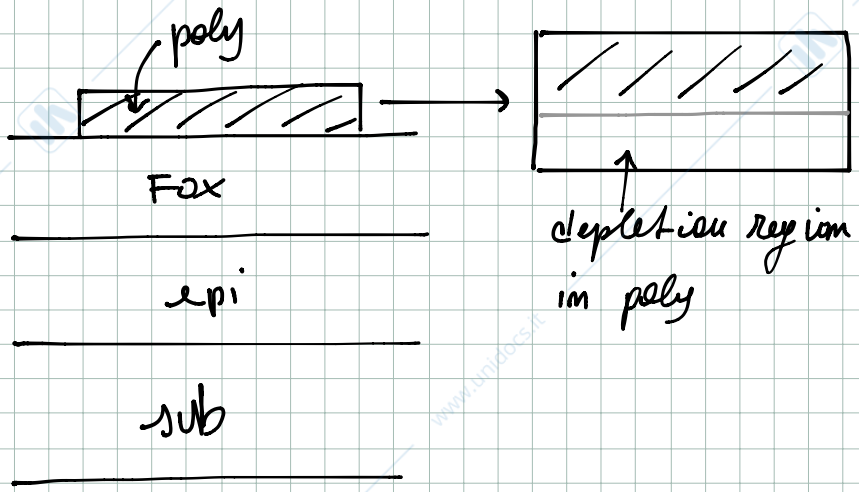
$k_T = +0,1\ \%/°C$

$\frac{\Delta R}{R} = 20\%$ still high

$Bc \hat{=} k_V \hat{=} 100\ ppm/V$ good

POLY_H RESISTOR

They have a big sheet resistance Rs



very affected by Vr,sub
By and Kv high
Effective resistance is limited by the effect of depletion region in poly

$R_S = 1 \div 10\ k\Omega/\square$

$\frac{\Delta R}{R} = \pm 30\%$

$k_T = -0,3\%/°C$

$B_C \cong k_V = 100\ ppm/V$