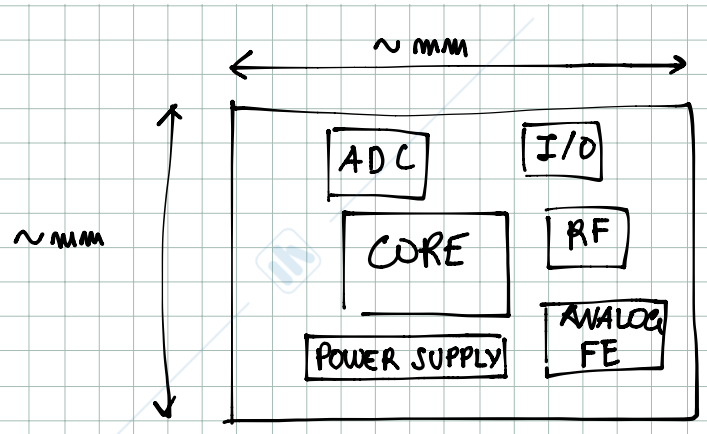
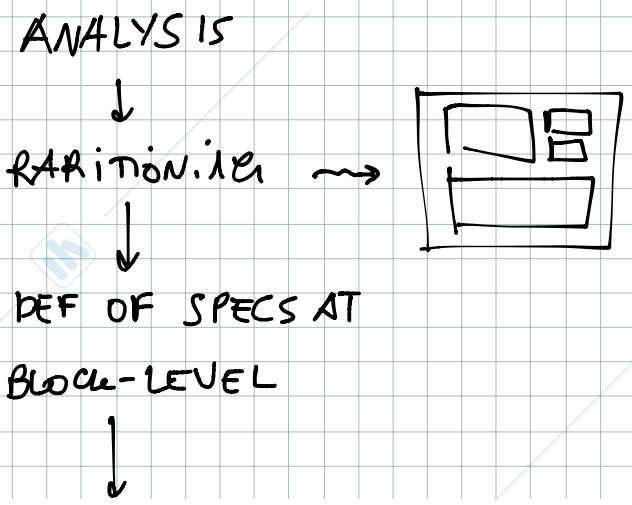
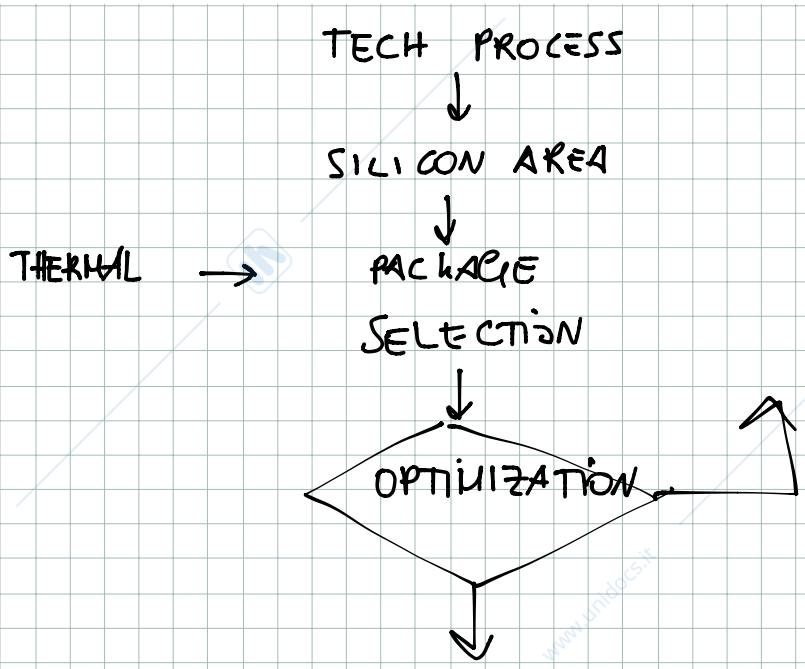



Main problems
- built precise circuit whith bad components
- isolate every functional block of a single chip. Every block is in the same d Silicon die and everyone can affect the others
-problems of package and its mechanical aspects

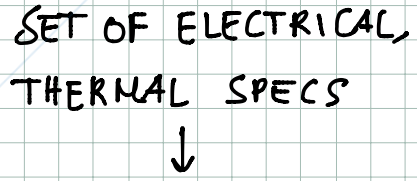
Design flow

We begin with specs and we start analyzing that and decide how we can divide every functional block (partitioning) .After we define every specs of every block (block level specifications) . Once defined that we have to decide the technological process trough we can satisfy the function asked, is to say, decide spathe set of components used.This selection affect the area of the chip that is the main part of costs of the whole work.
Finally we select the type of package taking into account thermal effects.
The we start optimizing the design may be repeating all the steps several times.

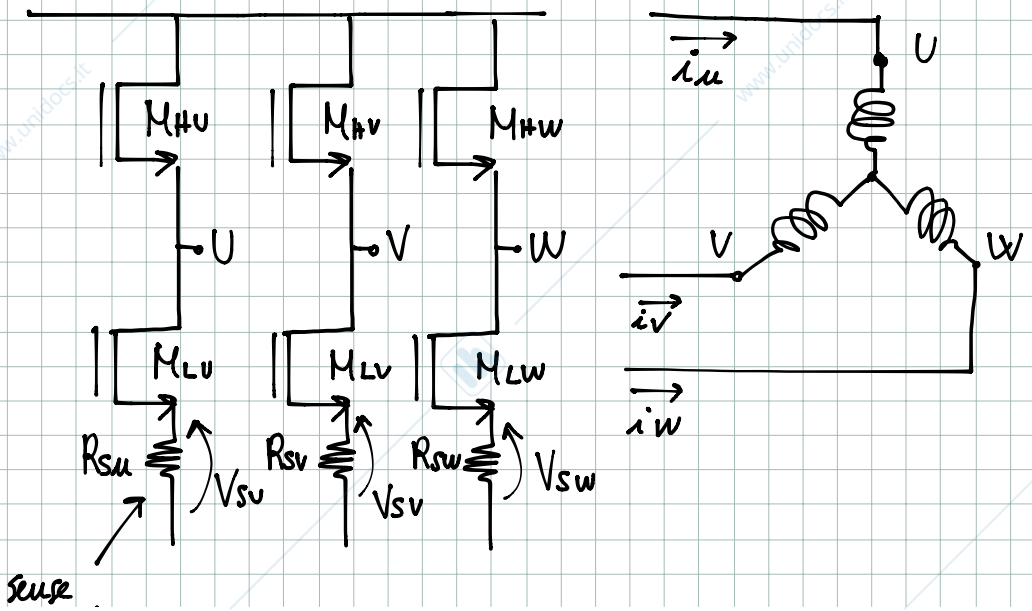


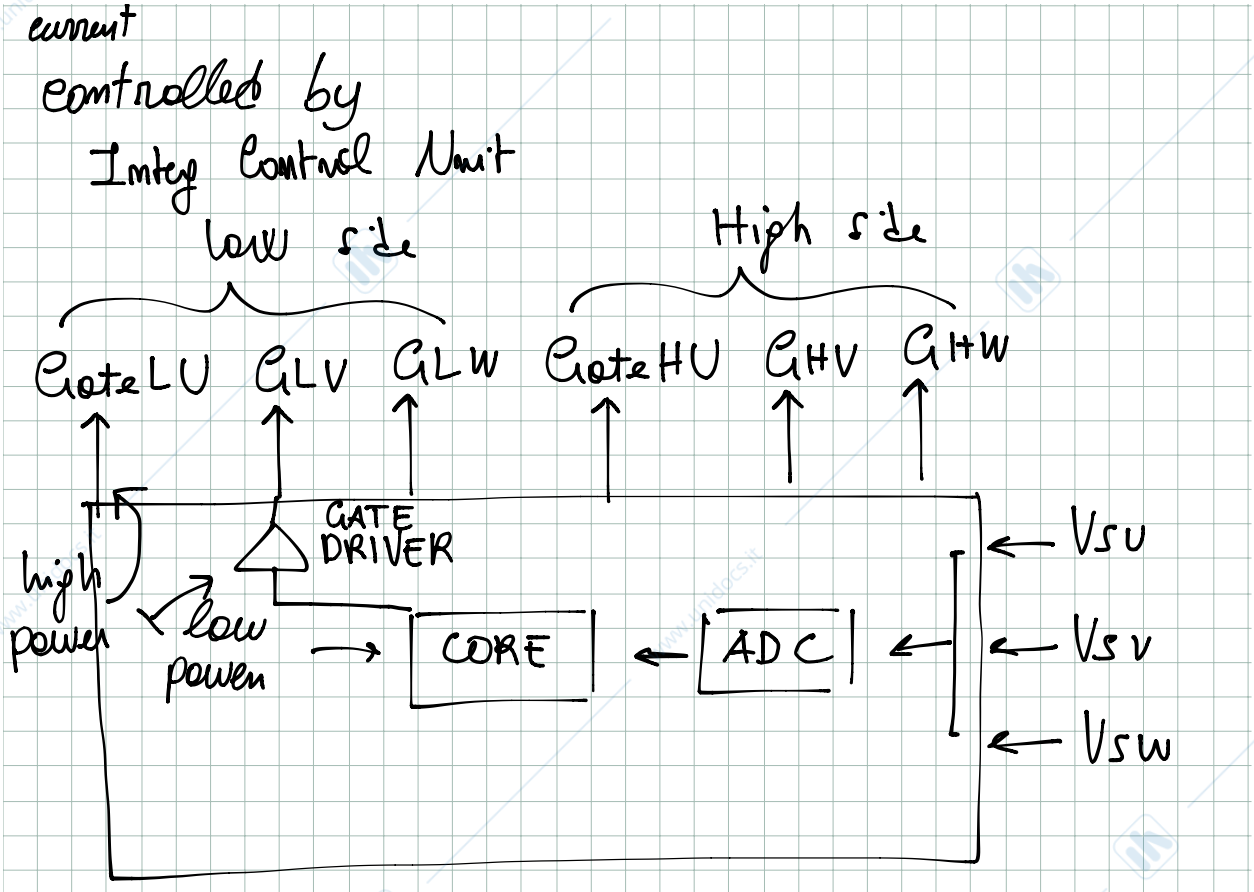



analog design flow

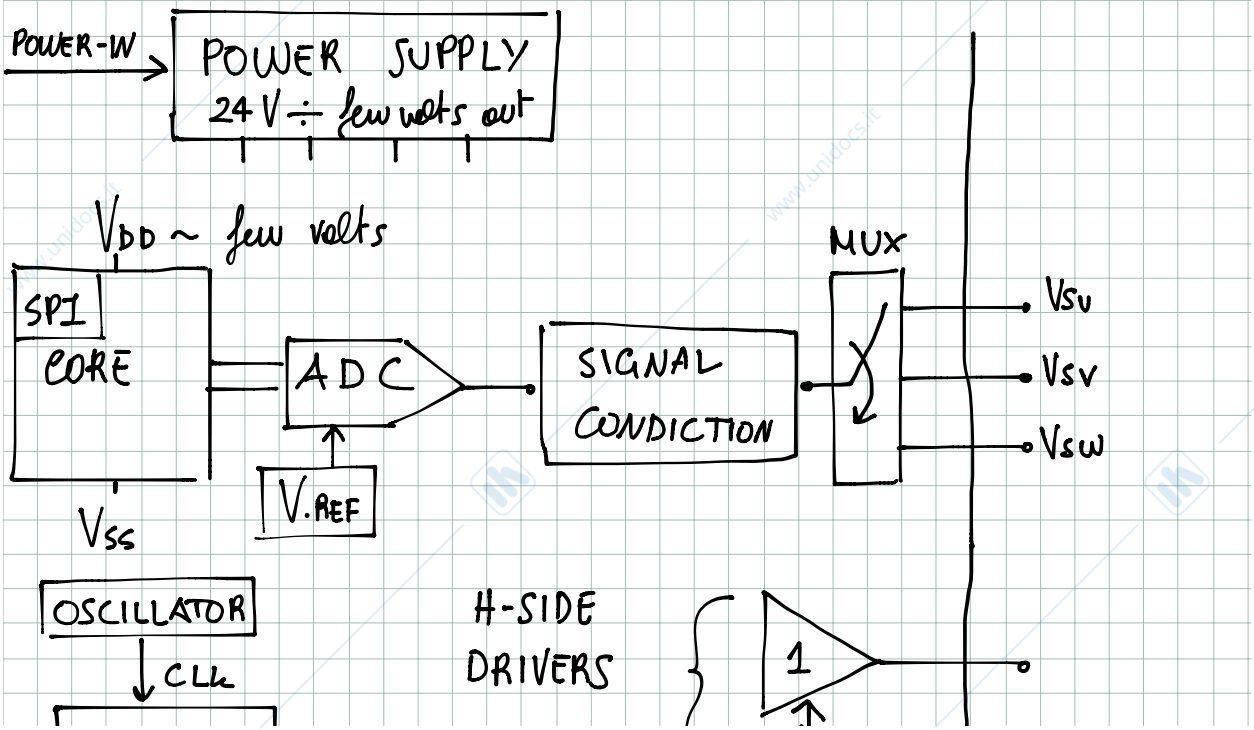


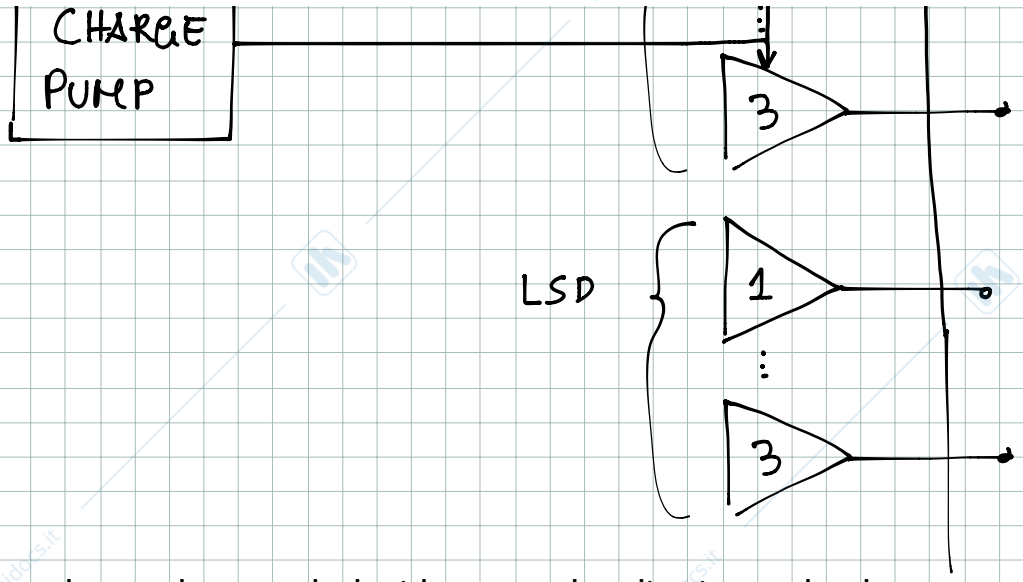

Example of dividing of blocks:
sensorless motor drives (we can only sense electrical quantities)






So we have to divide blocks

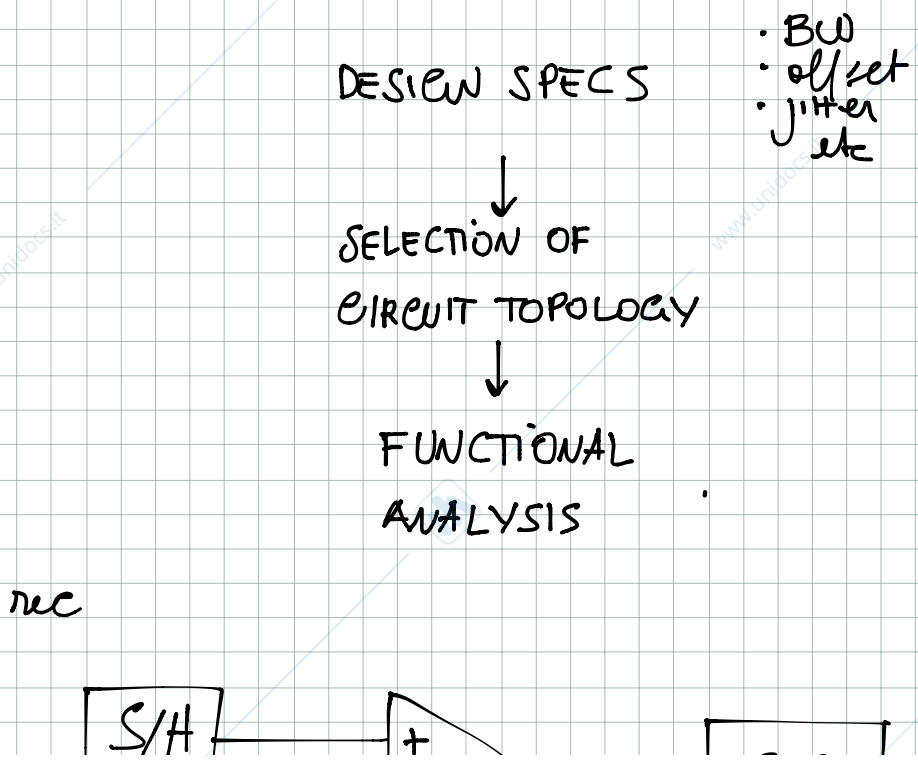


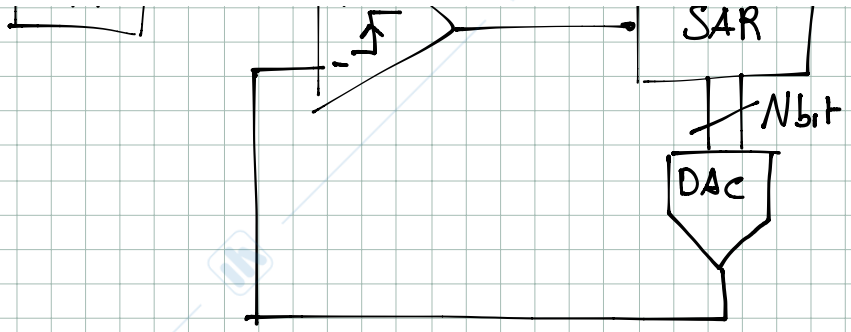



After that we have to deal with area and realization technology
Silicon area affects the cost

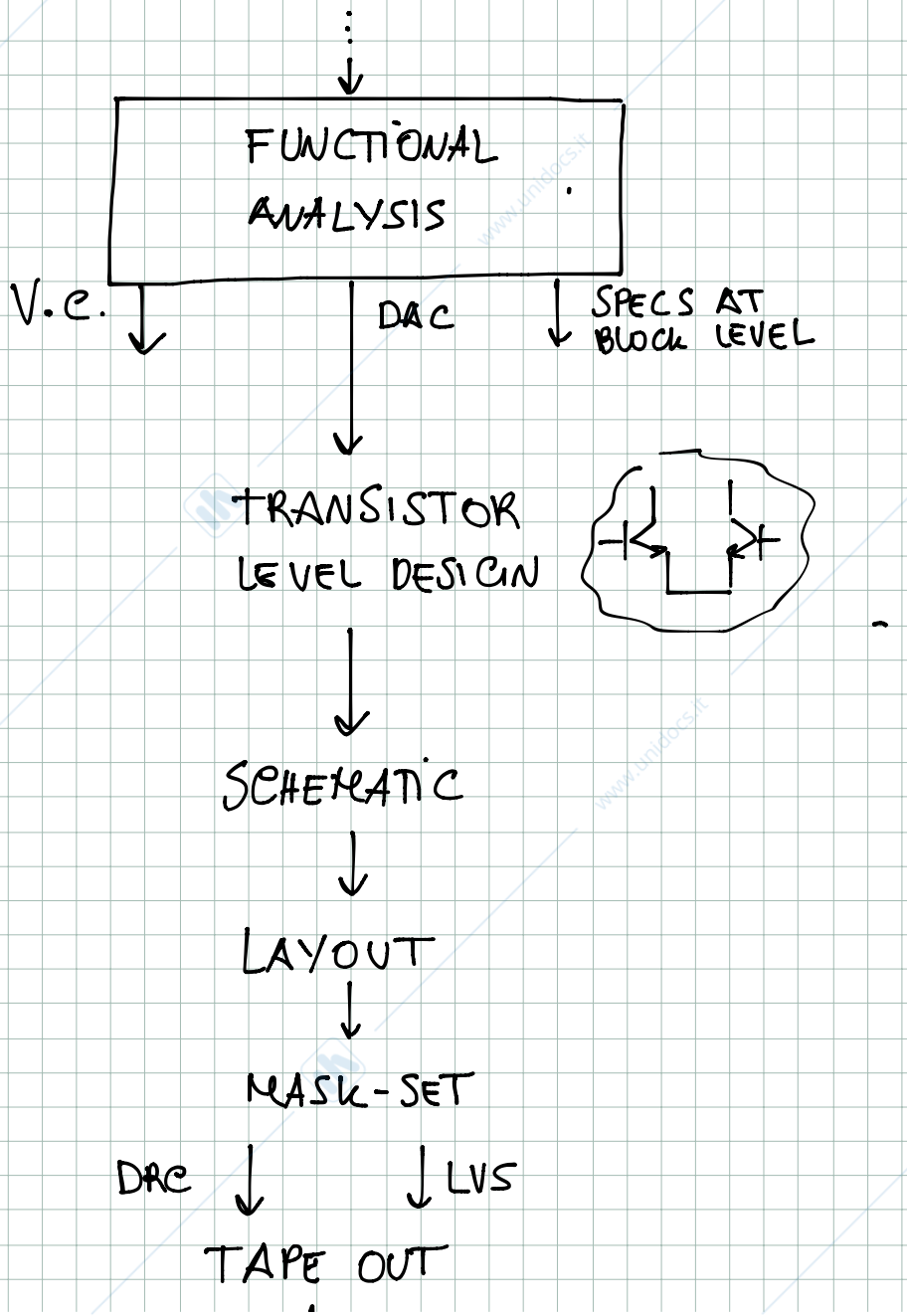
Tech lonely give us the design kit:
For example with CMOS tech we have
nMos , pMos , R C and BJT

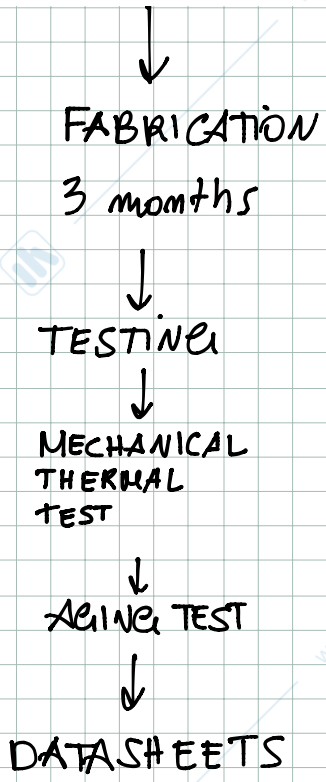
Analog design flow






We have to choose every specs of every part of the circuit, (rec)






Course program

1. Review design kit components
2. Fabrication tolerances
3. Review of basic building blocks
4. Design of OTA - OP AMPS
5. Voltage current references
6. Oscillators
7. PLL

Books

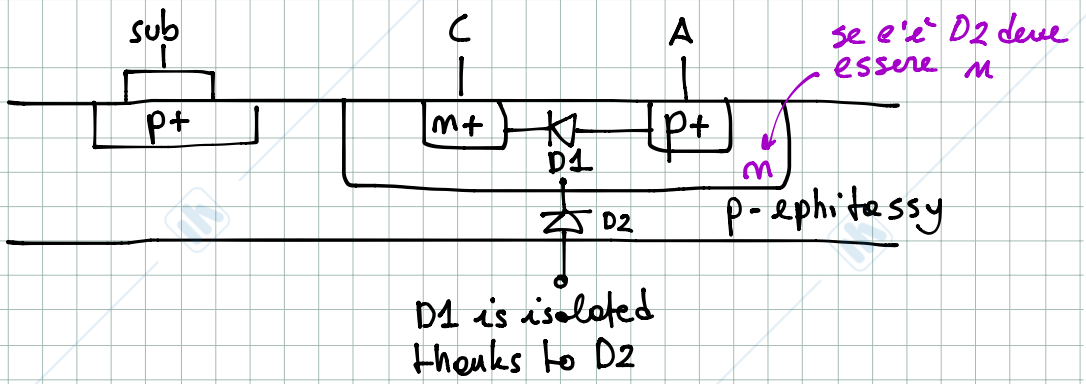
1. Analysis and design of analog ICs, Gray , Meyer - Wiley Ed.
2. Design of analog CMOS ICs , Razavi

CMOS TECHNOLOGY PPROCESS

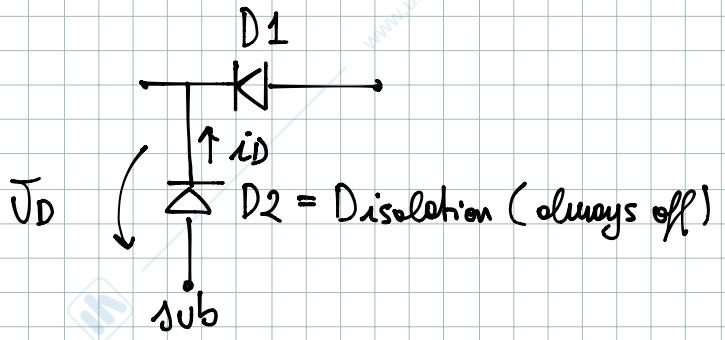
1. -voltage class
2. -components
3. isolation type .Thousands of transistors on the same silicon die
   A. Bulk
   B. SOI

A. BULK

Esm. Diode in CMOS




lowest potential p-sub



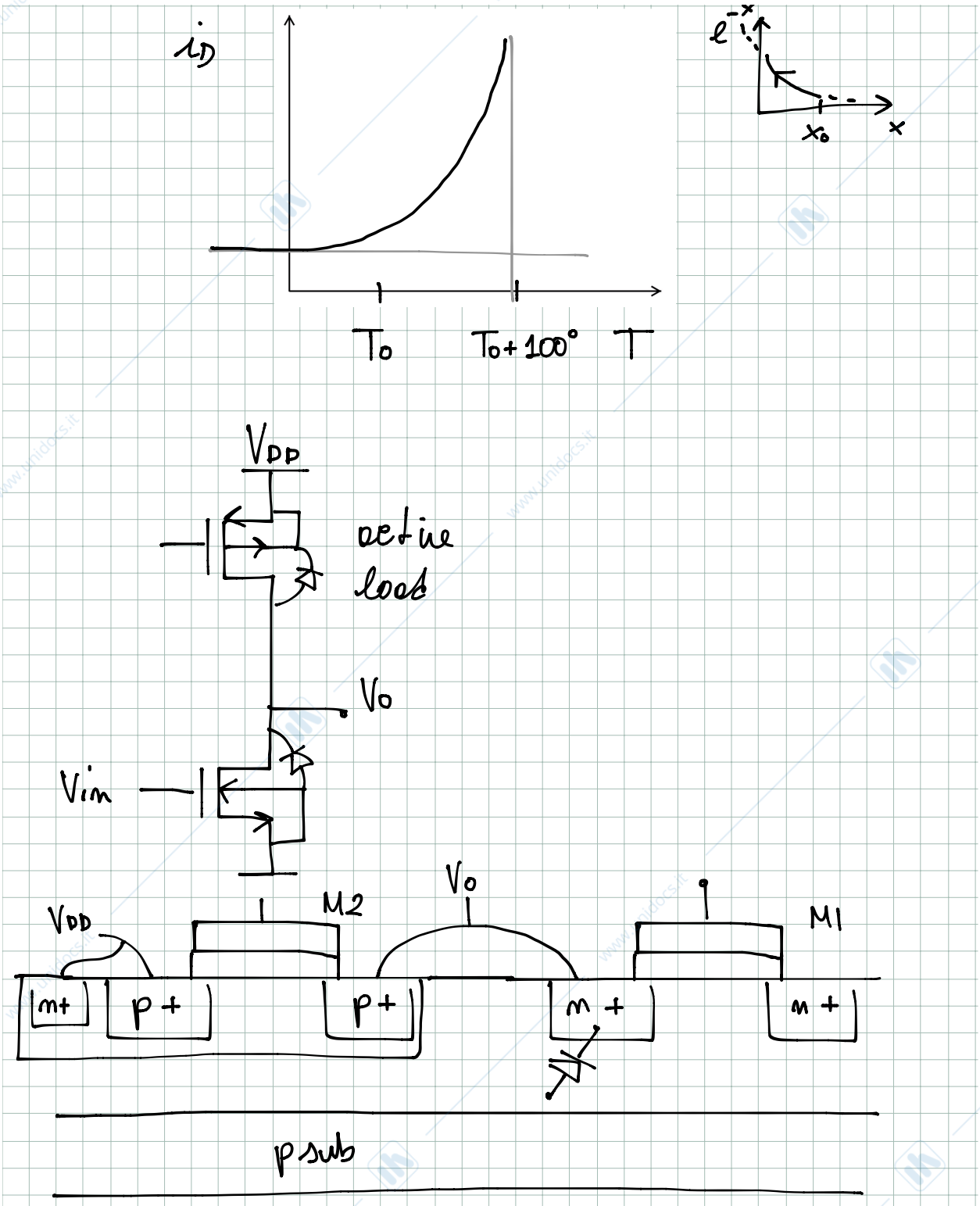

Critical aspects of Diso

Eq of a diode: $i_S \cong I_S \left[ \exp\left(\frac{J_D}{n V_T}\right) - 1 \right]$

$$V_T = \frac{k_B \cdot T}{q}$$

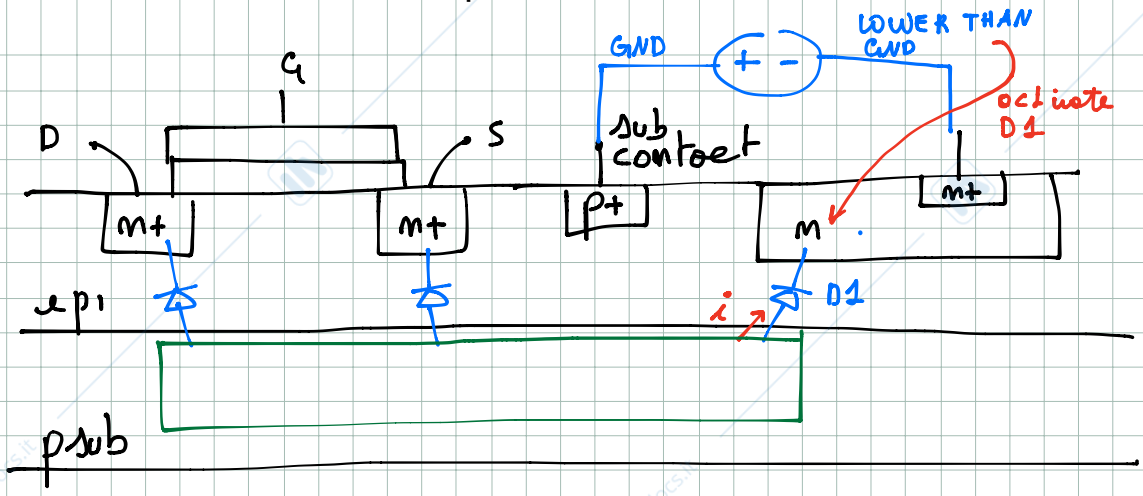
$$I_S = E\, T^{(4-m)} \exp\left(-\frac{V_{Ge}}{V_T}\right)$$

E: costant on temp

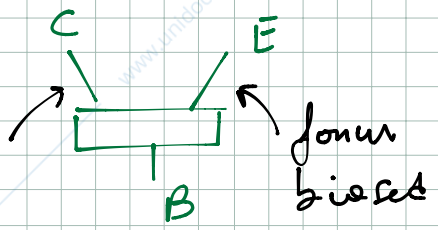


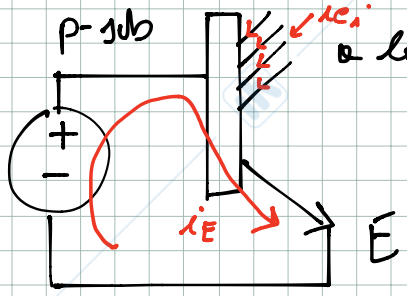

We have to take into account the leakage currents of the diodes

BULK tech suffers of activation of parasitics elements




it becomes a BJT



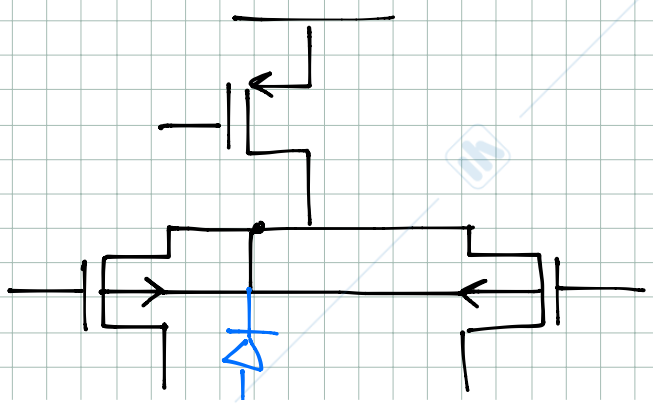



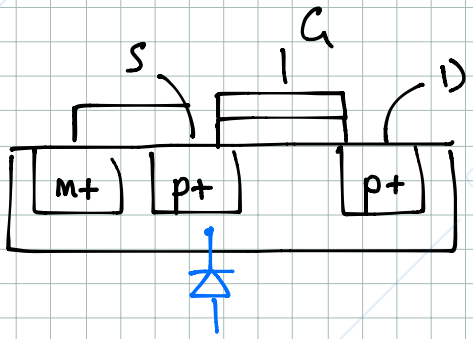

a lot of collectors

$\Rightarrow \beta \cong 10^{-3} \Rightarrow$

if $i_E = 1A \Rightarrow i_{C_1} = 1mA$

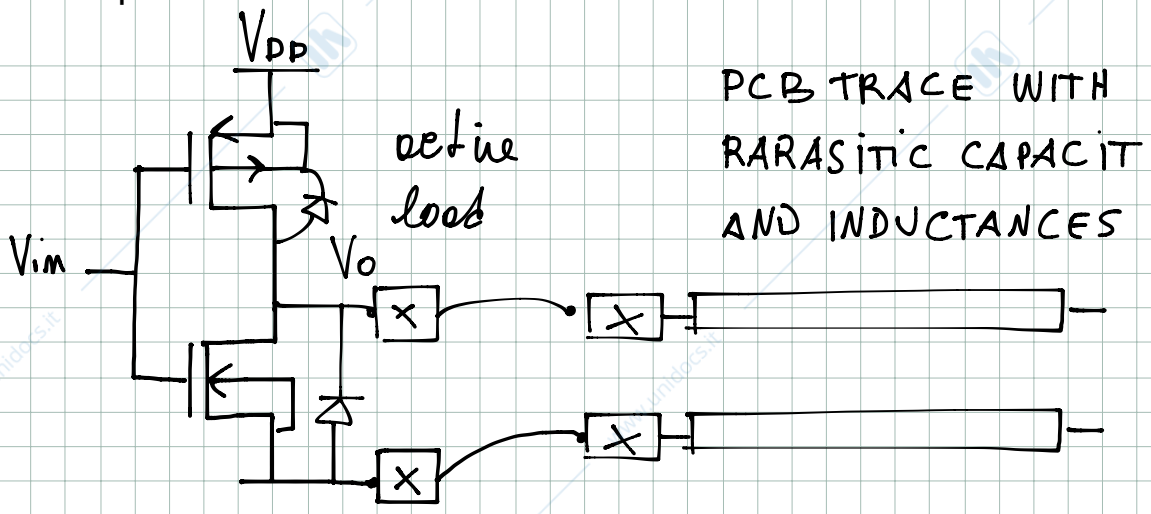
one of that $i_{C_1}$ can be :



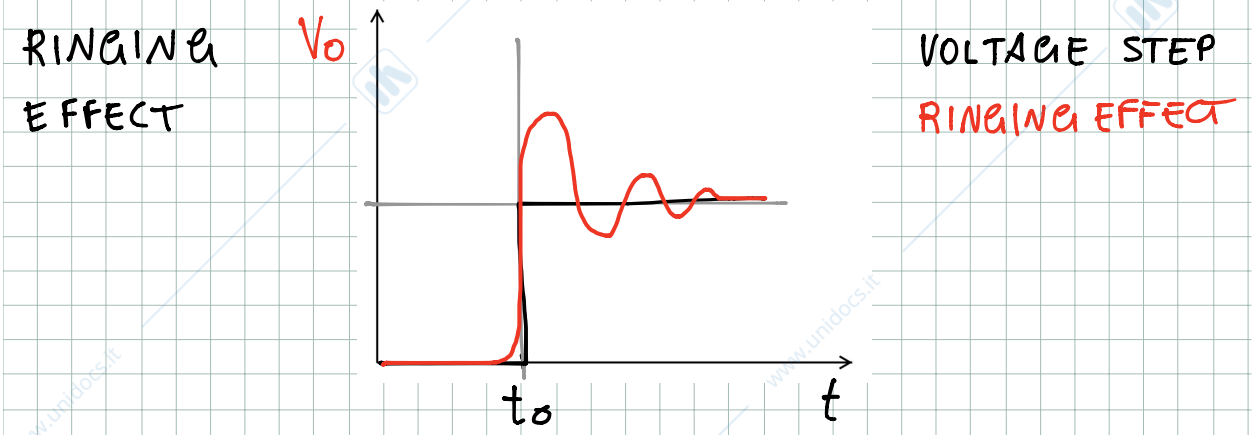


The result is that isolation layers are highly consumed by parasitics currents. The designer has to consider this scenario.

How that potential can be lower than GND?



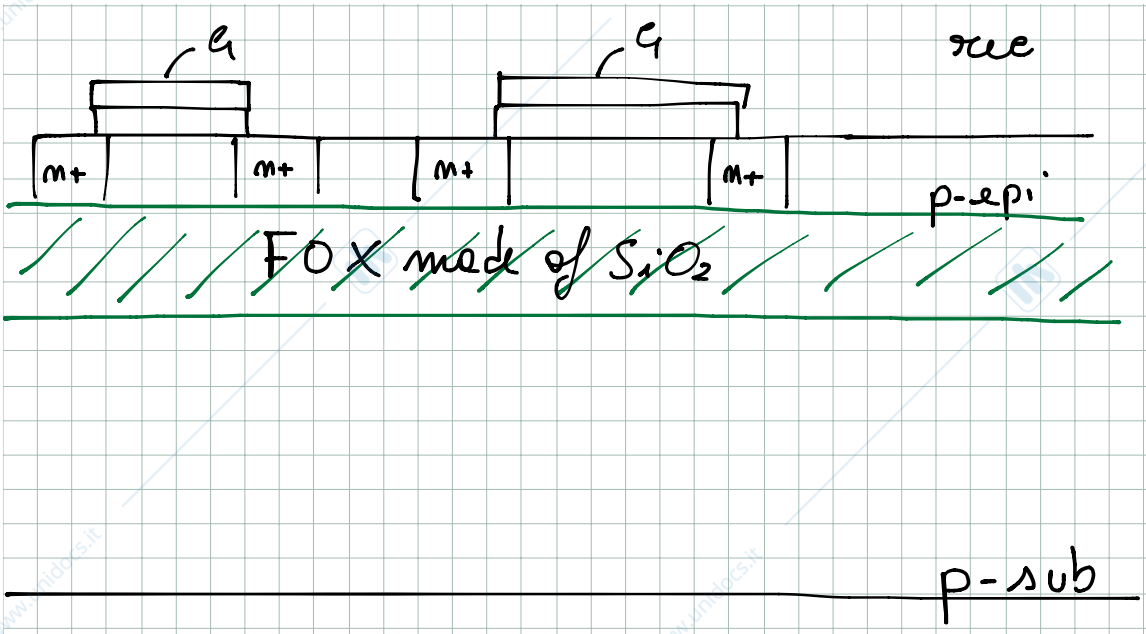

The parasitic capacitance and inductance of the PCB Trace can cause ringing Vo if a step voltage is applied at the PCB itself.




The latch-up problem is not the only one. This kind of technology also have huge parasitics capacitances. To solve both problems it was introduced a:

## JUNCTION ISOLATION TECHNOLOGY (JIC)

Consists of a film of oxide (FOX) that isolates the substrate from the "active part" of the circuit




drawbacks:

- Power dissipation is worse because FOX is an electric insulator but also a THERMAL INSULATOR
- Cost
- Parasitics transistors

Because if that drawbacks this technology is only used in specific applications