Resistors classification

Resistors

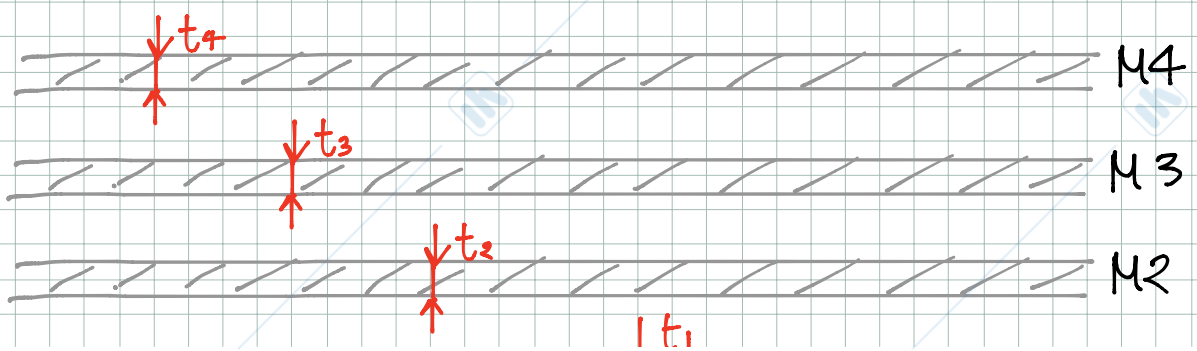
	R_S [Ω/□]	$\Delta R/R$ [%]	k_T [ppm/°C]	β_c ppm/kV
n-well	1k ÷ 20k	± 30		
n^+ diff	20 ÷ 80	± 20		
n^+ poly	20 ÷ 80			
poly_h	1k ÷ 20k			

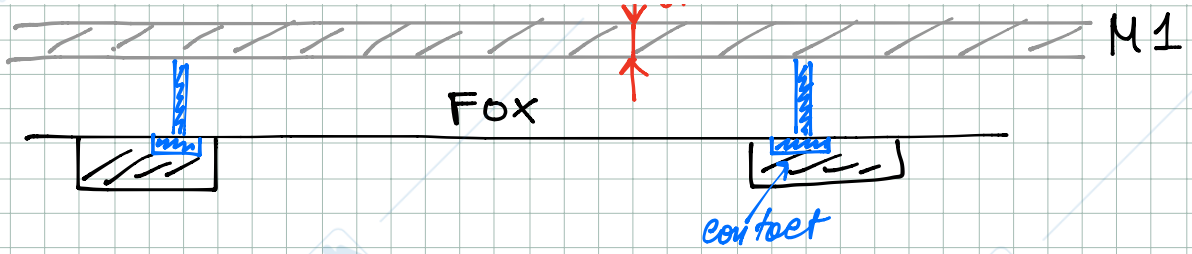
key parameters for now

Passive components: res, cap and interconnects

Interconnects

We have a bench of 5 or 4 metal layers . Some are connected to the silicon

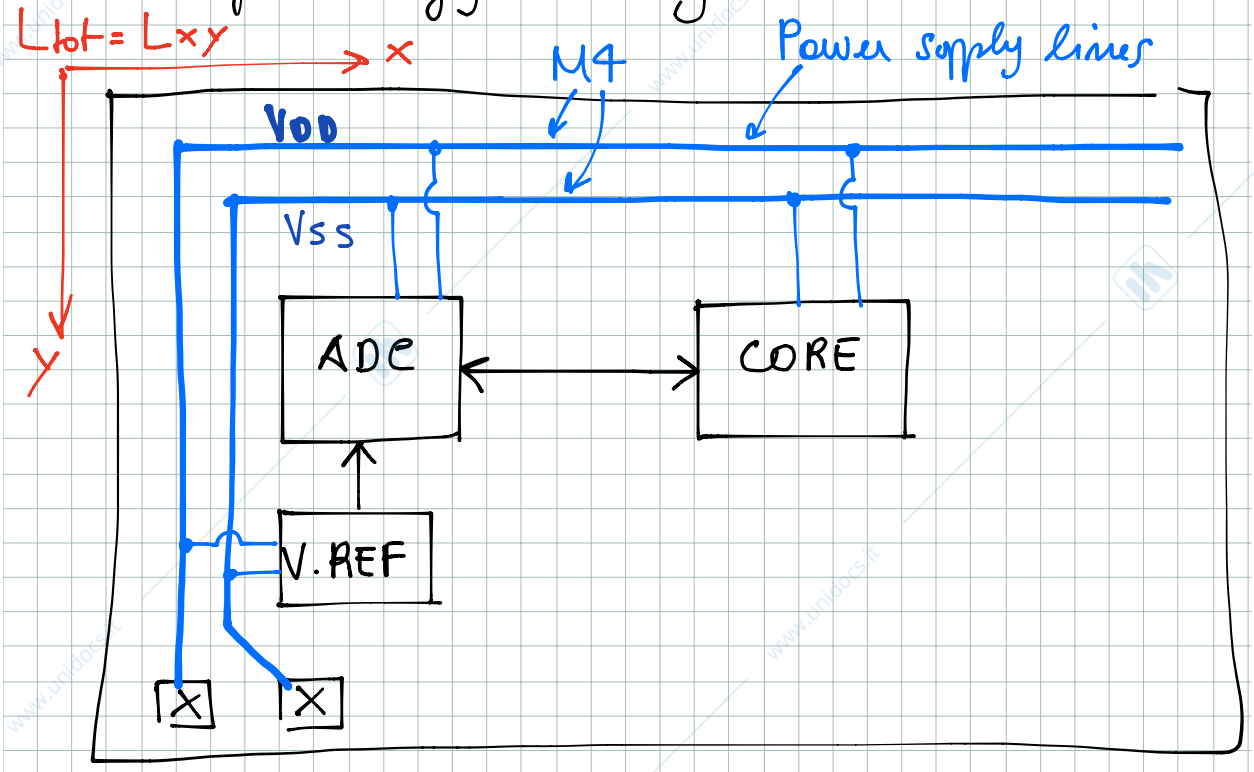




M1 is for local connections

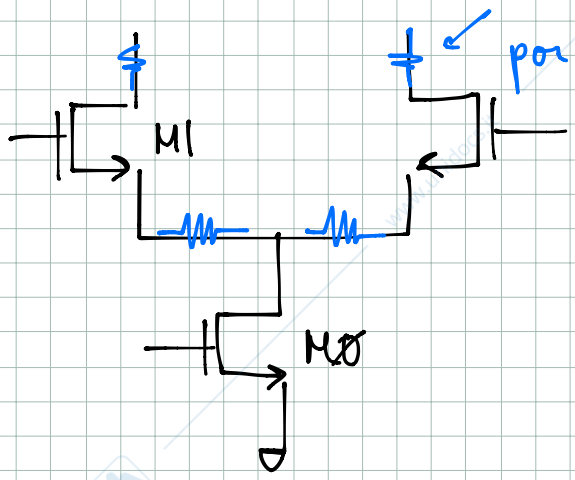
M2 is for block connections

M4 is for energy delivery

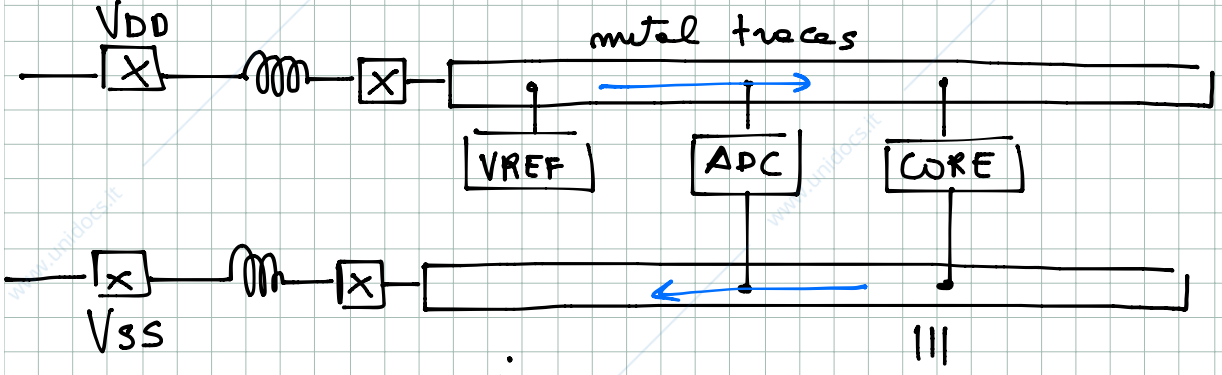


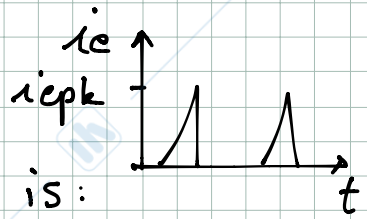
M1	50 ÷ 100	mΩ/□
M2	40 ÷ 80	"
M3	10 ÷ 30	"
M4	3 ÷ 10	"

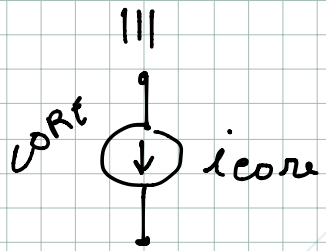
So we increase area going from M1 to M4 hence increase res going from M4 to M1.
Resistance of interconnection has to be maintained as low as possible (ideally zero).
The non-zero resistance of interconnections can interfere with the "nominal" behaviour of the circuit



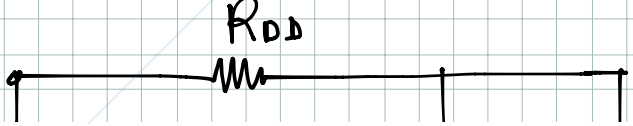
PCB level

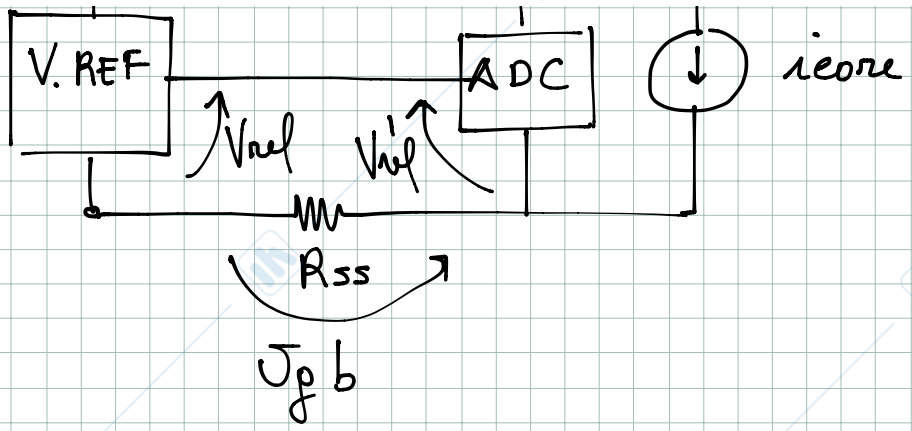






the situation is:





Vgb can be comparable with Vref:

with (M1): $R_S = 100\ m\Omega/\square$

$L_{xy} = 2\ mm$

$W = 5\ \mu m$

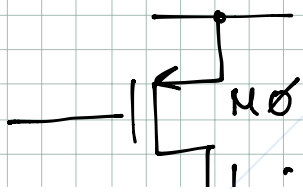
$i_{eore,pk} = 10\ mA$

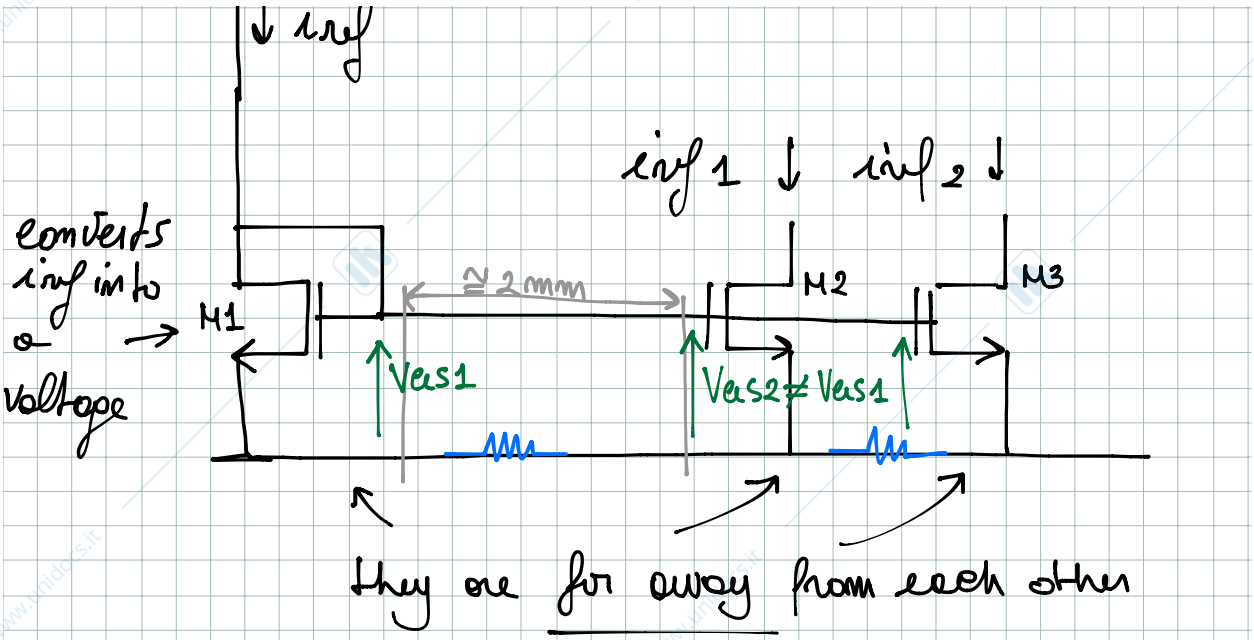
$\Rightarrow R_{SS} = 40\ \Omega \Rightarrow V_{gb} = 400\ mV$

So we have to keep low the impedance of metal interconnections

How about block connections?
Distance like: 2 mm

Effect on current references





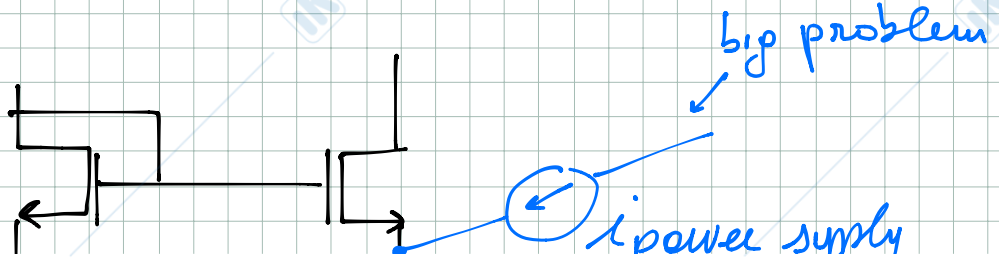
so parasitics resistance of interconnections makes the mirroring factor not to be perfect:

$$\frac{inf_1}{iref} = \frac{\mu_n \frac{C_{ox}}{2} \left(\frac{W}{L}\right)_0 (V_{GS} - V_{TH})^2}{\mu_n \frac{C_{ox}}{2} \left(\frac{W}{L}\right)_1 (V_{GS_2} - V_{Th})^2}$$

we can simplify because tech process is the same

that can't be simplified

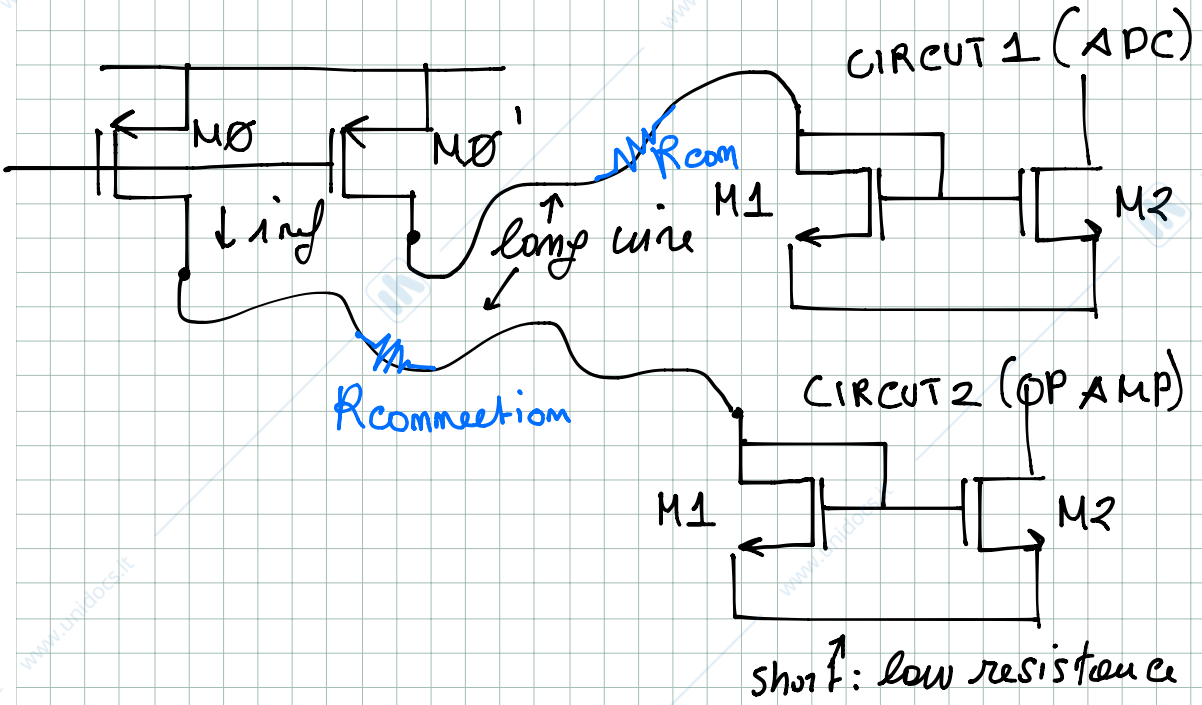
the solution is:



generated by other blocks like the core

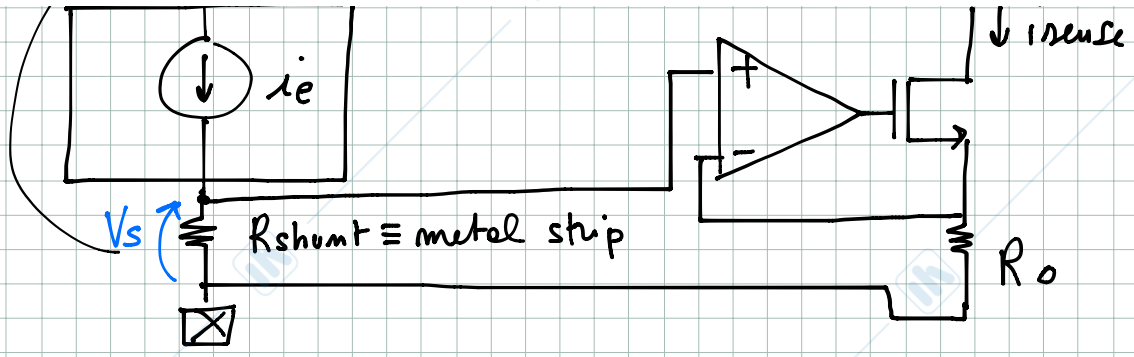
Parasitics currents generates a drop over Rss
So this kind of current mirror is not used for for away block but only for very local and close part of the circuit

One way to provide inf to other blocks is



"USING" resistance of interconnections

in some cases resistance of interconnections can be exploited to design some part of the circuit , using that resistance like a part of our circuit:
for example to measure the current flowing into a block



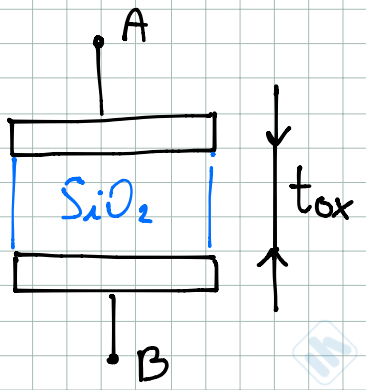
$$i_{sense} = \frac{V_s}{R_0} = \frac{R_s}{R_0} \cdot i_e$$

to make the sensing circuit to does not consume too much power we have to put

$$R_0 \gg R_s \quad like \quad \frac{R_0}{R_s} = 10^3$$

the ratio between Rs and R0 has to be the much costant as possible so they have to be made of the same material and be close one to the other to react the same way at temperature modifications. As Ro has a big value the sensing circuit does consume a lot of area.

Capacitors



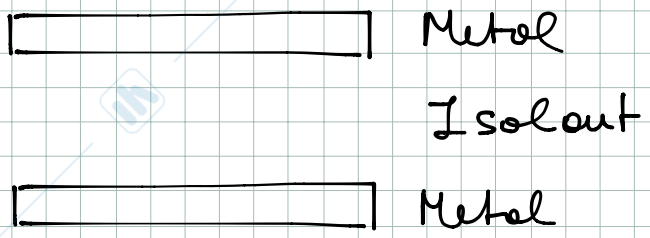
$$C = \varepsilon_0 \varepsilon_r \frac{W \cdot L}{t_{ox}} = C_{ox} W L$$

Main parameters for choosing a capacitor

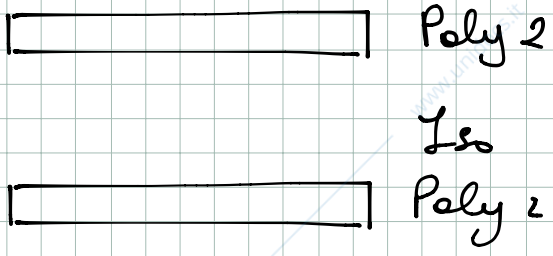
Cox

the bigger is that the lower the area is needed to reach a capacitance value.

MIM Cap



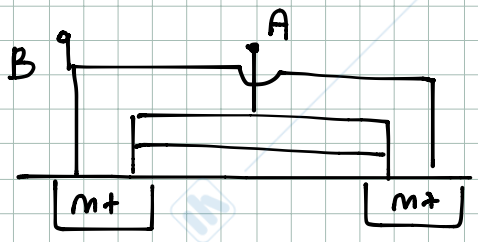
PIP cap



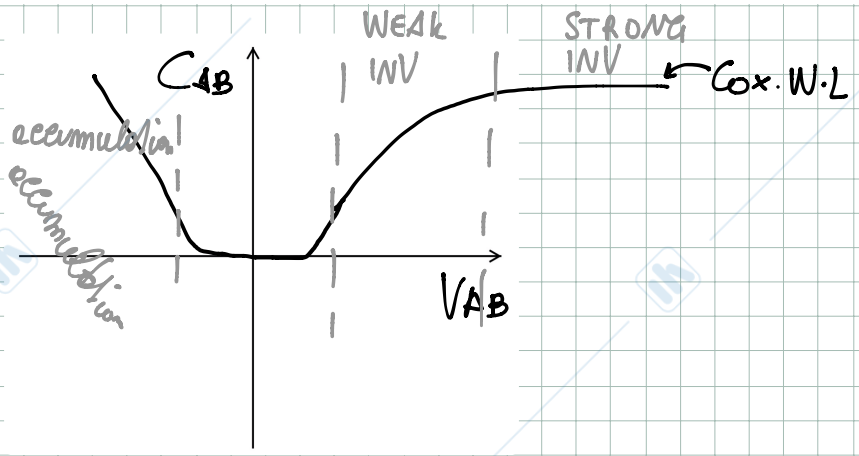
$10^{-2}\ fF/\mu m^2 < C_{ox} < 10^{-1}\ fF/\mu m^2$

Breakdown voltage

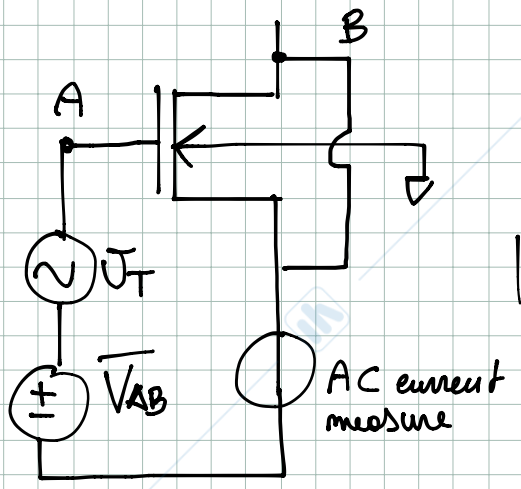
MOS CAP



Is thinner but the drawback is:



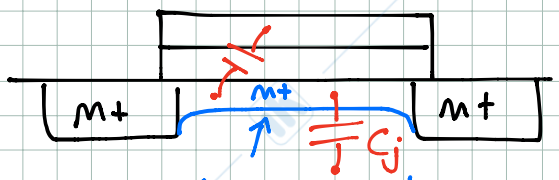
Is a non linear capacitor
Let's examine in detail:



$$C_{ox} \cong 4\ fF/\mu m^2$$

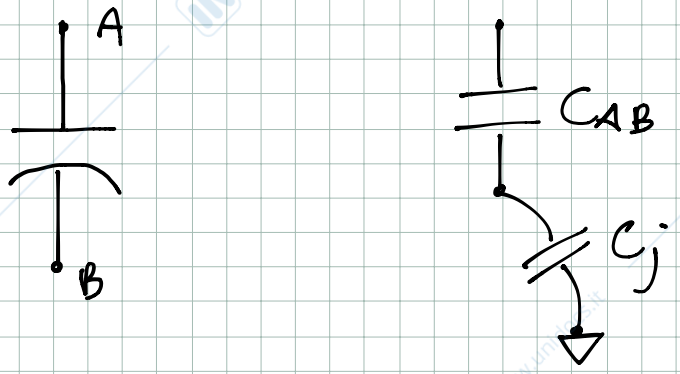
$$|Z_{AB}| = \left|\frac{V_g}{i_e}\right| = \frac{1}{\omega C_{AB}}$$

the other kind of capacitor are used to solve bad problems
To solve in part, the non linearity problem we fabricate like this:
At fab time we put an inversion layer lowering the voltage needed to make the mos work like a cap.

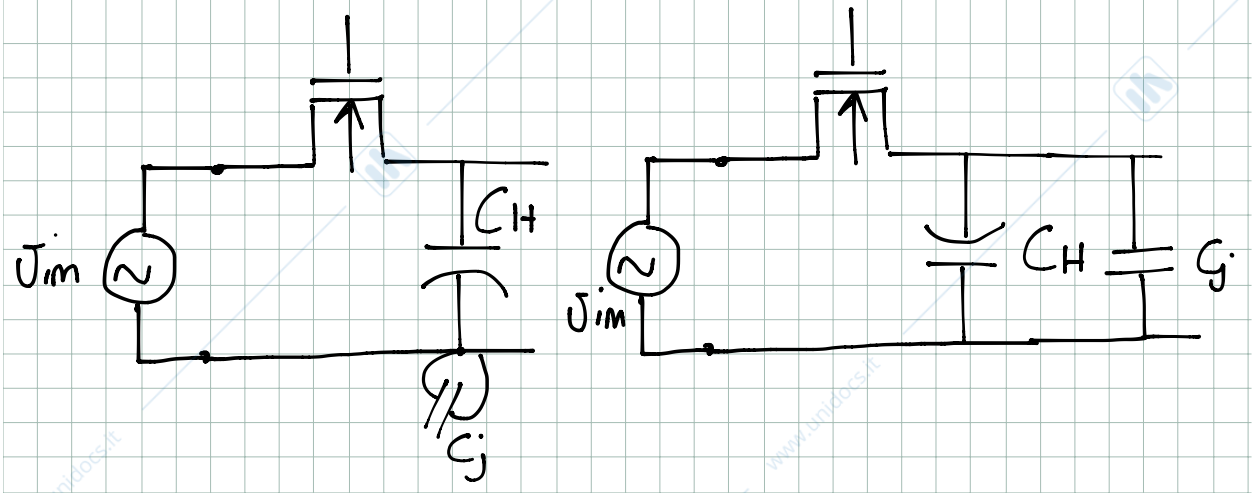


always present lowering the voltage needed to reach his wanted value

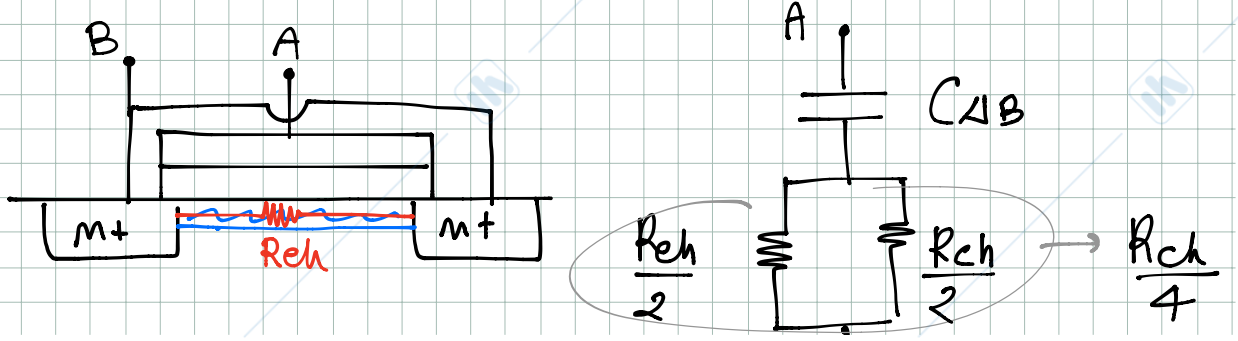
but it has a drawback: we have parasitics capacitance Cj so another parameter that classify the cap is Cox/Cj



these parasitics elects are not positive because the capacitor takes a verse of positioning. For example in a S/H circuit:



This kind of resistor have parasitics resistances that generates a time of constant for the charge of the resistor generating a bandwidth specification



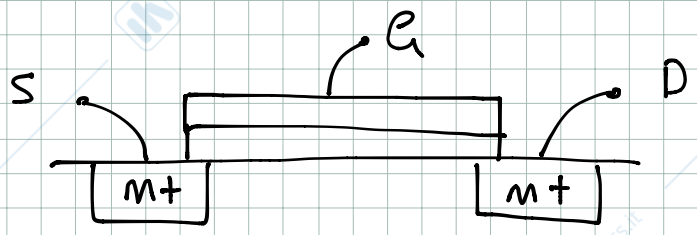
B

so the time constant is

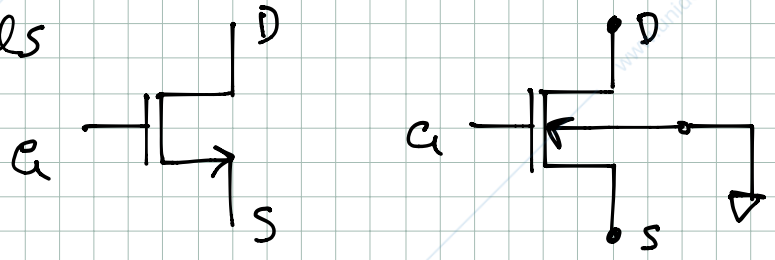
$$\tau = C_{AB} \cdot \frac{R_{eh}}{4} = \frac{C_{AB} W L}{4} \cdot \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{AB} - V_{th})^2}$$

$$= \frac{1}{4 \mu_n (V_{AB} - V_{th})} L^2$$

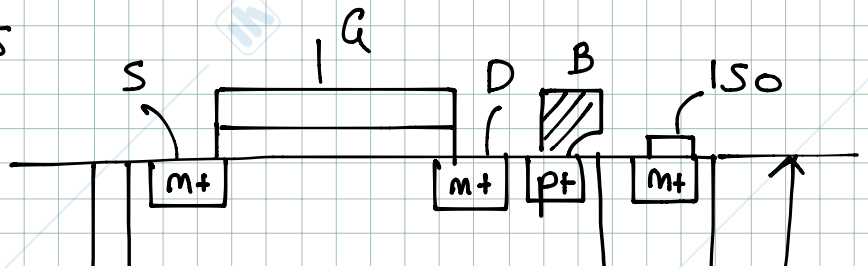
nMOS

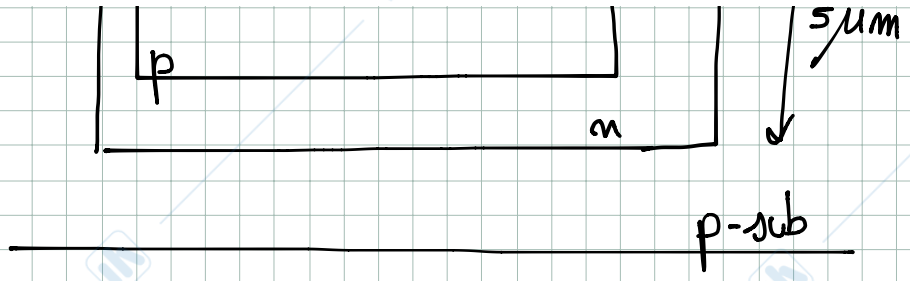


symbols

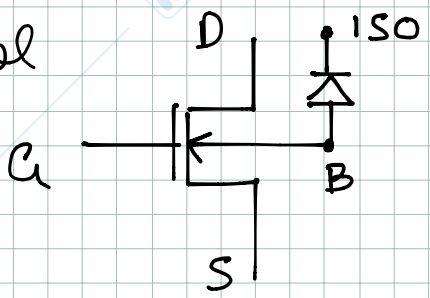


ISO MOS
closed

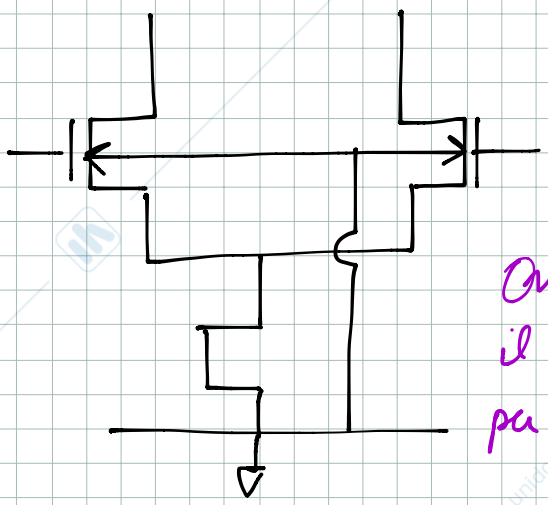




symbol



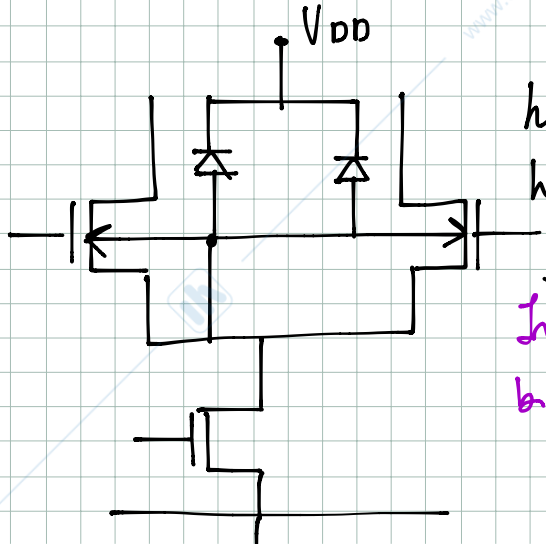
isolation effects



here we have body effect

Qui dobbiamo collegare il body a massa per evitare il latch-up?

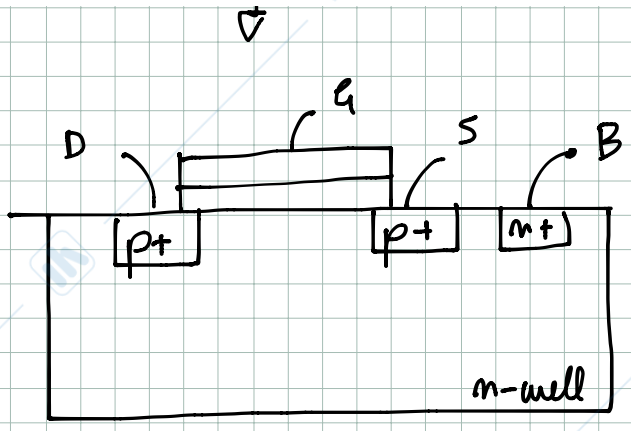
with iso

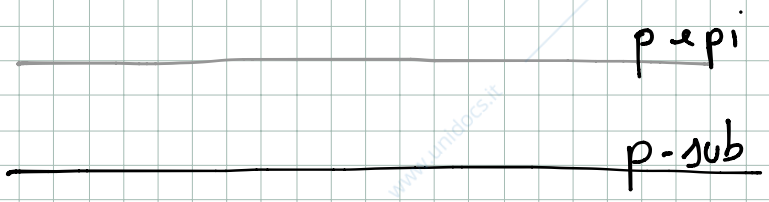


here we don't have body-effect

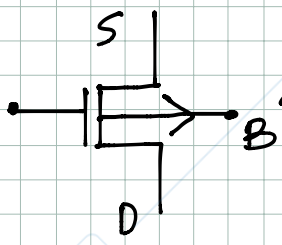
Invece qui non c'è bisogno

pMOS



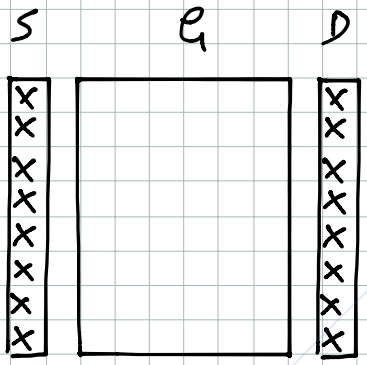


symbol



we can connect it in order to have or not body effect

Fabrication tolerances



Fabrication tolerances can effect alignments of contacts and shape of contacts making some parameters of the mos variyng

for example, in this expression:

$$i_D = \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{th})^2$$

$2\left(\frac{L}{\ldots}\right)$

tolerances affects C_{ox}, W, L, V_{th}

but there is an advantage. When two components very close are fabricated at the same time they are affected by the same tolerance errors. This is a very good thing because we can built circuits in order to "cancel the same tolerance".
For example, if we have two resistor fabricated together

$R_1 \neq R_{1\,nominal}$ $\quad R_1 = R_{1m} + \Delta R_1$

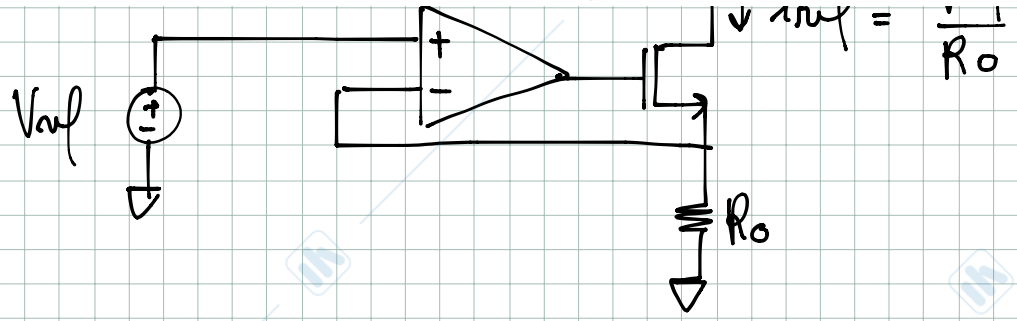
$R_2 \neq R_{2m}$ $\quad R_2 = R_{2m} + \Delta R_2$

and $\quad \frac{\Delta R_1}{R_{1m}} \cong \frac{\Delta R_2}{R_{2m}}$

so we can cancel tolerance in this way

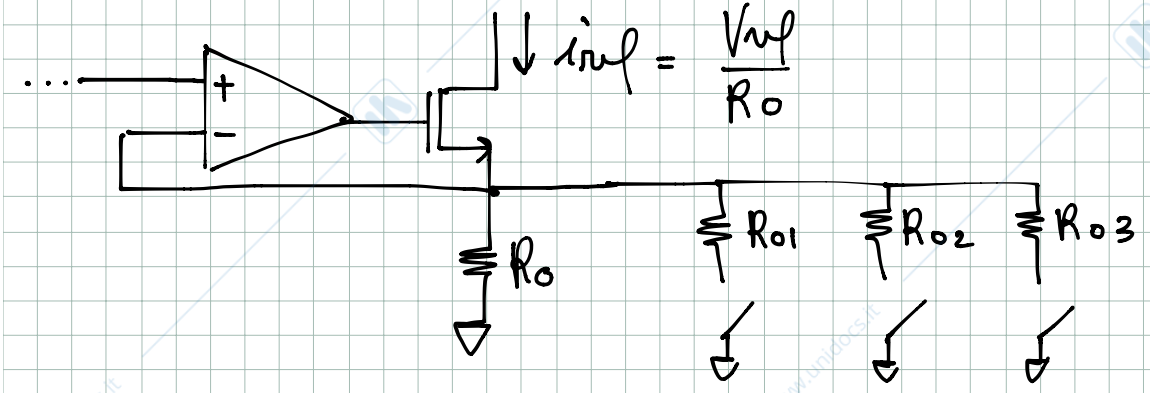
$$\frac{R_1}{R_2} = \frac{R_{1m}}{R_{2m}} \frac{\left(1 + \frac{\Delta R_{1m}}{R_1}\right)}{\left(1 + \frac{\Delta R_{2m}}{R_2}\right)}$$

When we have to transfer a voltage to a current we deal with transresistances



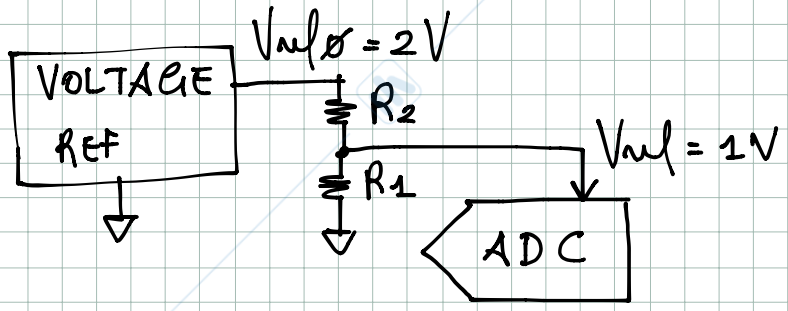
in the exp $\frac{V_{ref}}{R_0}$ we have no a ratio of quantities that can cancel the toler error. So an unique way to make the

circuit work properly is to TRIM every sample that is fabricated.
A way to TRIM this circuit is:



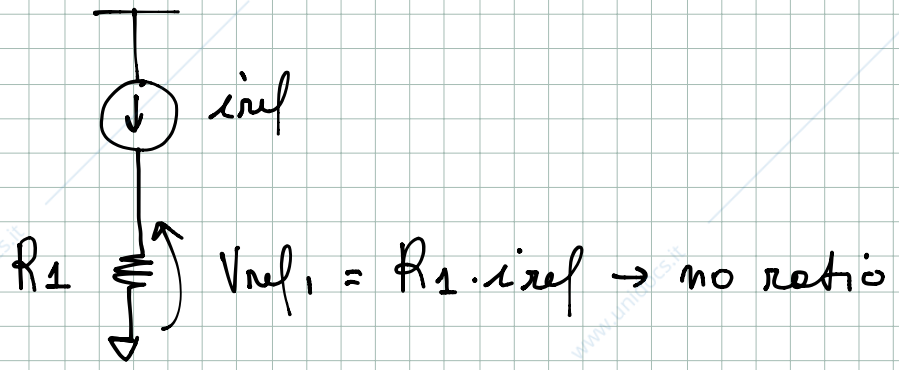
we will close or leave opened the switches in order to achieve a resistor value that makes the circuit to work.

Example

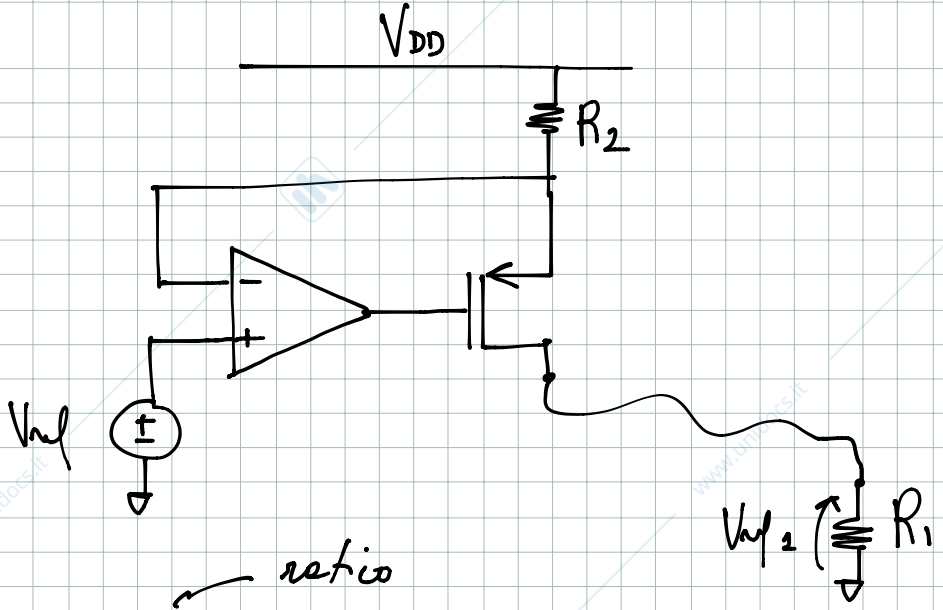


$$\frac{V_{ref1}}{V_{ref2}} = \frac{R_1}{R_1+R_2} = \frac{1}{1+\frac{R_2}{R_1}} \leftarrow \text{ratio!}$$

Sometimes the reference quantity is a current



But if we realize like this:



$$V_{ref1} = \frac{R_1}{R_2} V_{ref} \quad \text{(ratio)}$$

MISMATCH

We can express mismatch between two resistance with this eq:

$$M \qquad \frac{R_1 - R_2}{\cdot 100}$$

$$\frac{\Delta T}{T} = \frac{}{\frac{R_1 + R_2}{2}} \cdot 100$$

Or either with this:

$$\Delta = \frac{\frac{R_2}{R_1} - \frac{R_{2m}}{R_{1m}}}{\frac{R_{2m}}{R_{1m}}} = \frac{R_{1m}}{R_{2m}} \frac{R_2}{R_1} - 1$$

We will use this eq. because it involves ratio of quantities.

We have a lot of pairs of resistor in the same silicon die, so we can calculate mismatches for everyone:

$$\Delta_1, \Delta_2, \dots, \Delta_N$$

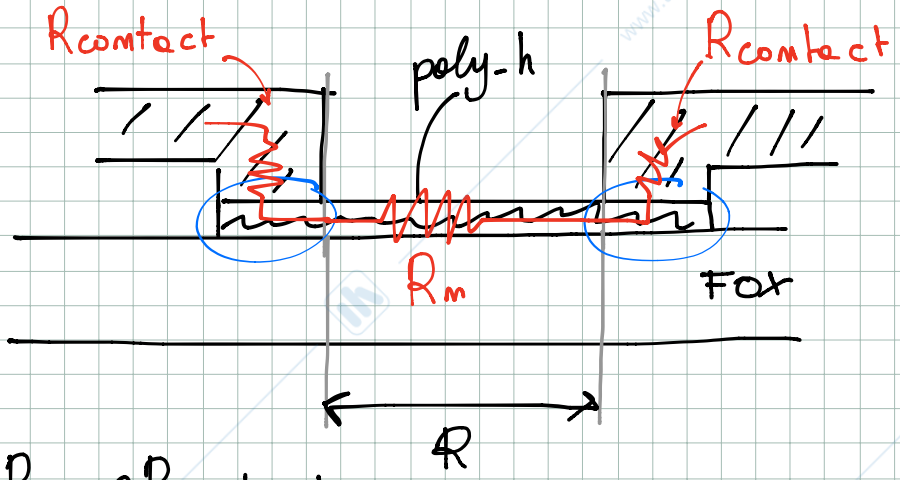
SYSTEMATICAL MISMATCH

$$m_\Delta = \frac{1}{N} \sum_{i=1}^{N} \Delta_i$$

RANDOM MISMATCH

$$S_\Delta = \left[\frac{1}{N-1} \sum_{i=1}^{N} (\Delta_i - m_\Delta)^2 \right]^{\frac{1}{2}}$$

Let's apply this eq to a poly_h resistor:



$$R = R_m + 2R_{contact}$$

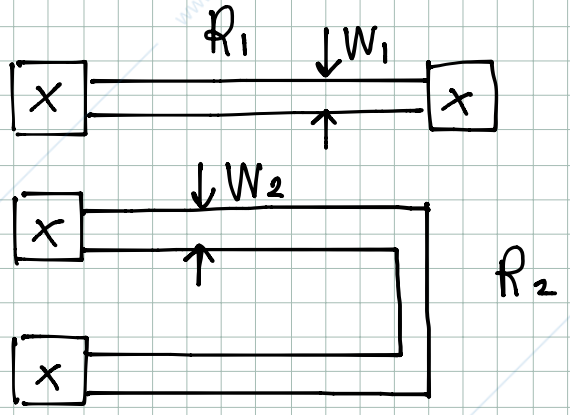
$$\Rightarrow \quad \int = \frac{(R_{2m} + 2R_{ctc})}{(R_{1m} + 2R_{ctc})} \cdot \frac{R_{1m}}{R_{2m}} - 1 =$$

$$= \frac{R_{2m}\left(1 + \frac{2R_{ctc}}{R_{2m}}\right)}{R_{1m}\left(1 + \frac{2R_{ctc}}{R_{1m}}\right)} \cdot \frac{R_{1m}}{R_{2m}} - 1 \neq 0$$

Example

$R_{1m} = 2k\Omega$

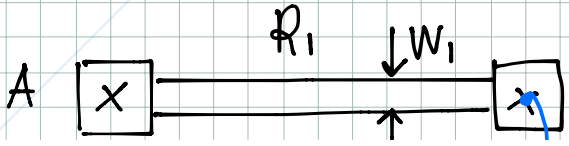
$R_{2m} = 4k\Omega$



$$R_2 = N R_1 \qquad N = 2$$

$$\int = \frac{R_2}{R_1}\frac{R_{1m}}{R_{2m}} - 1 = \frac{N R_1}{R_1}\frac{R_{1m}}{N R_{1m}} - 1 = 0$$

a way to cancel the fab tolerances in presence of Rctc is to connect in series two resistor in order to make a resistor of the double value, so R2 could be made in this way:



Random mismatches $S_\int$