Q&A 07/02/23

T1

a) ENUNCIATE THE ELMORE'S THEOREM AND THE CONDITION THAT MUST BE FULLFILLED TO BE VALID

CONDITION:

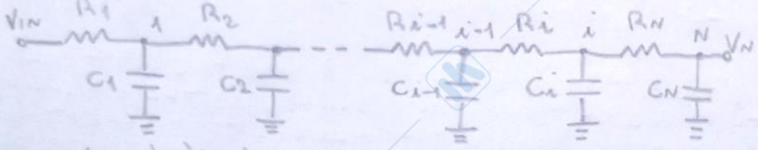
1- THE NETWORK HAS A SINGLE INPUT NODE

2- ALL THE CAPACITANCE ARE BETWEEN A NODE AND GROUND

3- THE NETWORK DOES NOT CONTAIN ANY RESISTIVE LOOP

THE ELMORE THEOREM ALLOWS TO ASSESS THE DELAY OF A NETWORK BY EVALUATING THE FIRST-ORD TIME CONSTANT OF THE NETWORK (WHICH IS EQUIVALENT TO THE FIRST MOMENT OF THE IMPULSE RESPON

b) APPLY THE THEOREM TO STIMATE THE DELAY OF A WIRE FEATURING A LENGTH L, A SPECIFIC CAPACITANCE PE UNIT LENGTH c' AND A SPECIFIC RESISTANCE PER UNIT LENGTH r'



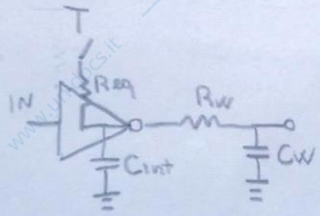
$\tau_{OUT} = CR + 2CR + 3CR + \dots + NCR$

$= \frac{N(N+1)}{2} CR$

WITH $C = \frac{C_W}{N} = \frac{c'L}{N}$ AND $R = \frac{R_W}{N} = \frac{r'L}{N}$

$\tau_{OUT} = \frac{N(N+1)}{2} \frac{c'L}{N} \cdot \frac{r'L}{N} = \frac{(N+1)}{2N} c'r'L^2$ FOR N LARGE $\tau_{OUT} \simeq \frac{c'r'L^2}{2} = \frac{C_W R_W}{2}$

c) ESTIMATE THE DELAY OF THE WIRE WITH A LUMPED MODEL ($R_W = r'L$ AND $C_W = c'L$) AND COMPARE THE RESULT WITH THE ONE OBTAINED ANSWERING THE PREVIOUS QUESTION



$\tau_P = \ln(2)\left[C_{int} R_{eq} + C_W (R_W + R_{eq})\right]$

THE LUMPED RC MODEL OVERSTIMATES THE DELAY SINCE WE GET A TIME CONSTANT RC, WHILE WITH THIS MORE ACCURATE MODEL THAT RESEMBLES A DISTRIBUITED LINE WE GET $\frac{RC}{2}$

T2

a) WHICH ARE THE THREE CONTRIBUTIONS TO POWER CONSUMPTION OF A DIGITAL CIRCUIT?

INSTANTANEOUS POWER, MAXIMUM POWER, AVERAGE POWER

b) TWO CONTRIBUTION DEPEND ON THE OPERATING FREQUENCY OF THE CIRCUIT. EXPLAIN BRIEFLY THEIR DEPENDANC ON THE FREQUENCY WITH WHICH THE CIRCUIT IS RUN

CONSIDER A SIMPLE RC NETWORK DRIVEN BY A VOLTAGE GENERATOR THAT TRANSITIONS ABRUPLY FROM 0V AND VDD AND LET'S EVAL THE ENERGY DISSIPATED BY THE GENERATOR ITSELF. SO $E = C_L \cdot V_{DD}^2$ IF THE CHARGING ENERGY OF THE CAPACITANCE IS REPEATED PERIODICALLY WITH A FREQUENCY $f_{0\to1}$, THE RELATED POWER CONSUMPTION IS $P = C_L V_{DD}^2 f_{0\to1}$

c) HOW DOES THE DOMINANT CONTRIBUTION TO THE POWER CONSUMPTION BEHAVE WITH THE TECHNOLOGY SCALING? CONSIDER THE OPERATING FREQUENCY CONSTANT

IS DEPEND ON THE SCALING AND INCREASE LINEARLY WITH ITS f_{CK} S BECAUSE THE SPEED OF CIRCUIT IS INCREASE

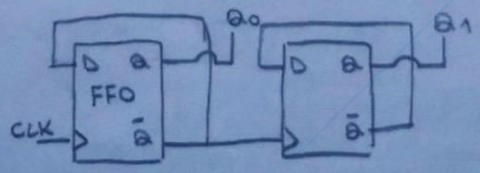
T3

a) WHAT IS THE MAIN VANTAGE OF AN ASYNCHRONOUS COUNTER WITH RESPECT TO A SYNCHRONOUS COUNTER? AND THE MAIN DOWNSIDE?

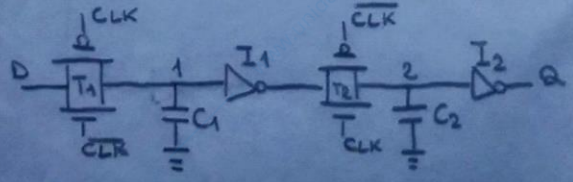
IN THE ASYNCRONOUSE COUNTER MAIN CLOCK IS ONLY APPLIED TO THE FIRST FLIP-FLOP AND THEN FOR THE REST OF FLIP-FLOPS THE OUTPUT OF PREVIOUS FLIP-FLOP IS TAKEN AS A CLOCK BUT THERE IS HIGH PROPAGATION DELAY

b) DESIGN A MOD-4 ASHINCRONOUS DOWN COUNTER USING POSITIVE EDGE TRIGGERED FLIP-FLOP

Q_1	Q_0
1	1
1	0
0	1
0	0



c) DESIGN A DYNAMIC POSITIVE EDGE-TRIGGERED D FLIP-FLOP



d) CONSIDER THE DESIGNED FLIP-FLOP, IMPLEMENTED IN THE REFERENCE INTEL 0,25 μm WITH ALL NMOS AND PMOS TRANSISTORS FEATURING AN ASPECT RATIO OF 3 AND 1, RESPECTI ASSUMING CONSTANT D INPUT AND A CLOCK RUNNING AT 2GHZ, ESTIMATE THE POWER CONSUM CONSIDER $\overline{CK}$ GENERATED BY AN IDEAL INVERTER

$$C_g^{(1)} = C_{int}^{(1)} = C'\left[\left(\frac{W}{L}\right)_n + \left(\frac{W}{L}\right)_p\right] L_{MIN} = 2fF$$

$$P = \left[\frac{3}{4}C_g^{(1)} + \frac{3}{4}C_g^{(1)} + \frac{1}{4}C_g^{(1)} + \frac{1}{4}C_g^{(1)}\right] V_{DD}^2 \cdot f = C_g^{(1)} V_{DD}^2 f = 50\,\mu W$$

TG

a) WHEN THE FIRST BIPOLAR TRANSISTOR WAS INVENTED? AND BY WHO?
1948 FROM WALTER BRATTAIN AND JOHN BARDEEN AND SHOCKLEY

b) WHO DESIGNED THE FIRST INTEGRATED CIRCUIT (IC)? TO BE HONEST TWO EXEMPLARES WE DIFFERENT ENGINEERS INDEPENDENTLY IN A SPAN OF 6 MONTHS. DO YOU REMEMBER WHEN THIS JACK KILBY AND BOB NOYCE IN 1958

c) IN THE BEGINNING THE FIRST ICs WERE MADE OF BIPOLAR TRANSISTORS, THEN IN 19 TRANSISTORS WAS DEVELOPED AND FROM LATE 1960S THIS KIND OF TRANSISTOR OVERWH THIS WAS DUE ALSO TO THE TECHNOLOGY DEVISED BY FEDERICO FAGGIN THAT ALLOWE MOS TRANSISTORS. WHAT WAS THE PROBLEM OF THE MOS TRANSISTORS AND WHAT TE FAGGIN PERFECTIONED THE SELF-ALIGN GATE TECHNOLOGY TO IMPLEMENT RELIABLE

d) WHAT DID GORDON MOORE STATE IN 1965 (THE FAMOUS MOORE'S LAW) AND THAT H THAN 5 DECADES?
EVERY 2 YEARS THE MINIMUM LENGTH OF THE TRANSISTOR WOULD SCALE-DOWN BY A FACT SING THE INTEGRATION DENSITY BY A FACTOR 2 (AREA SCALES BY A FACTOR 2)

e) WHAT KIND OF MOS TRANSISTORS ARE NOWADAYS USED BY THE MAIN SEMICONDUCT INTEL, SAMSUNG, TSMC, APPLE, BROADCOM?
P-MOS