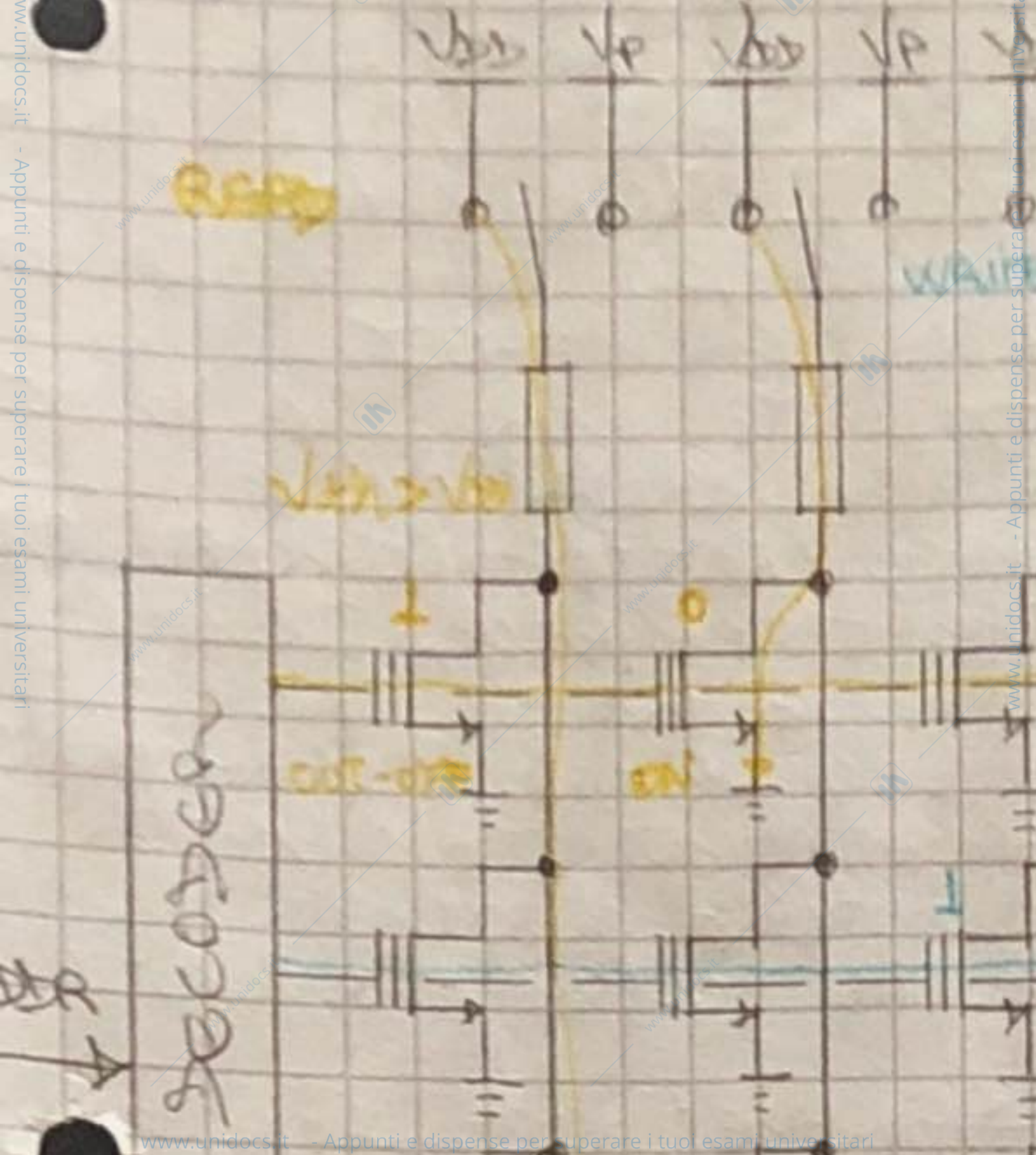
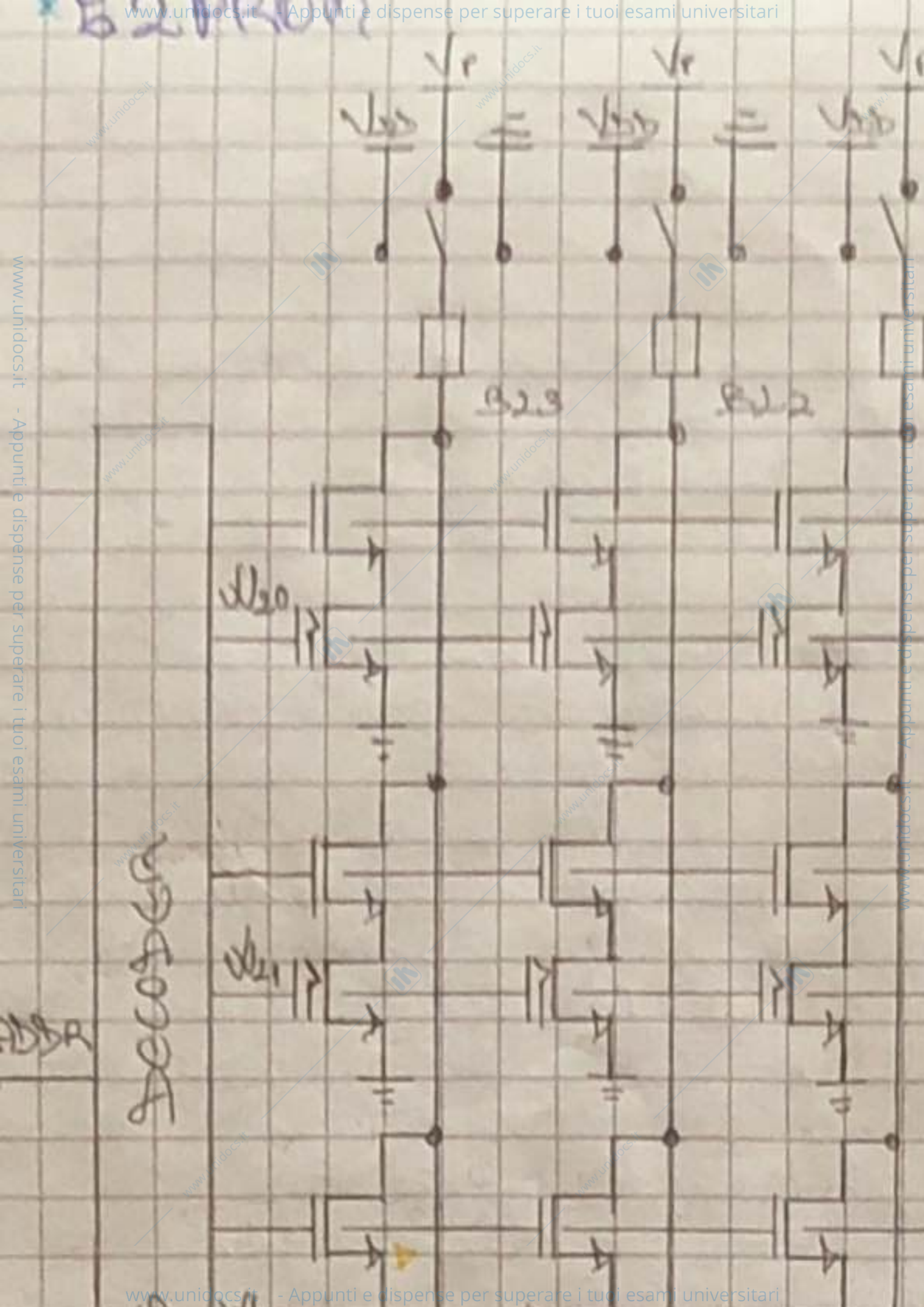
MEMORIES

EPROM





HOT ELECTRONS PRO[…]

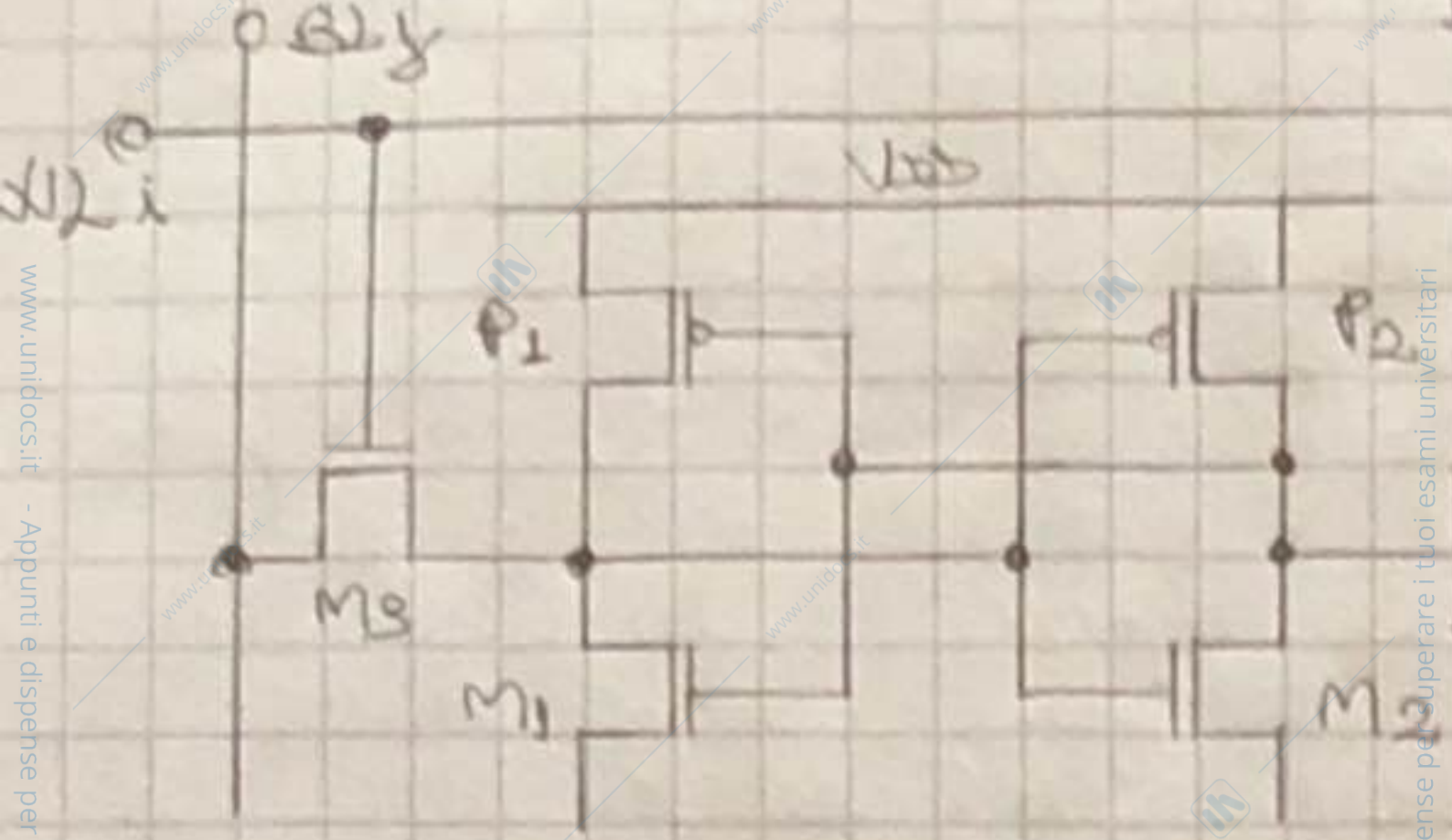
FAMOS TRANSISTOR A HI[…]
VOLTAGE $V_P \gg V_{DD}$ IS APPLI[…]
CHANNEL. ANOTHER HIGH V[…]
DRAIN AND SOURCE, CRE[…]
ACCELERATES ELECTRONS […]
EFFECT, SOME ELECTRONS […]
THE OXIDE (SiO_2) BARRIER[…]
THEY ARE TRAPPED TO REM[…]
GONE ONTO THE CIRCUIT […]
TRANSFER ENOUGH ENERGY[…]
SUBSTRATE.

TUNNELING/FOWLER-N[…]

TRANSISTORS TO MOVE ELE[…]
IDE, EITHER DRAIN OR […]
TO GATE WITH DRAIN GROUND[…]
IN THE INT PASS THE BARR[…]
PHENOMENON OF TUNNELING[…]
REVERSE VOLTAGES, I.E. […]
REMOVE ELECTRONS OF […]

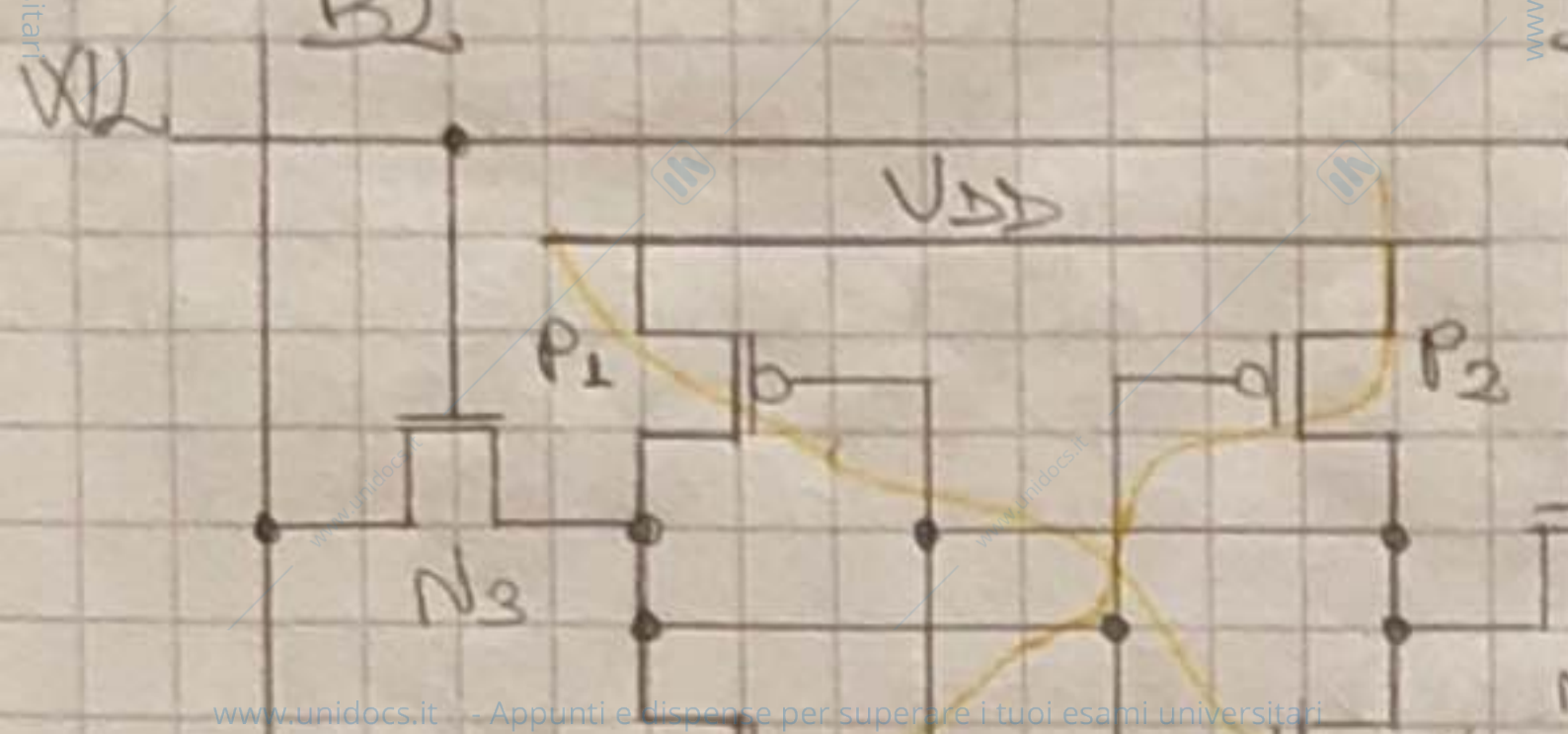
NO[…] E[…]

SRAM



QUESTION 13

CAM



→ MATCH: A2. WORD
CHANGING BIT LED.S CO
TO VDD, AND BIT LINES
AND ITS COMPLEMENT
• WHEN DATA IS
0. N5 IS ON AND N6 IS O
IS AT 0, SO Nt IS OFF AN
RESULTING IN A HIT.
• WHEN 1 AND 1
S CONNECTED TO B2 AT
• WHEN 1 AND 0
IS AT 1, SO Nt IS ON
N A MISS.
• WHEN 0 AND 1,
S B2 AT 1, RESULT IS

CACHE

→ DIRECT MAPPING:
STORES IN THE SAME
FIELDS, THE LOWEST
WITHIN A LINE. THE MAP

DRAM ACCESS

→ FAST PAGE: AFTE
NEW OPERATION CAN B
S, CHANGING THE ADDRE
OLUMN, AND THEN REACT
ONE NEED TO BE CONTIG

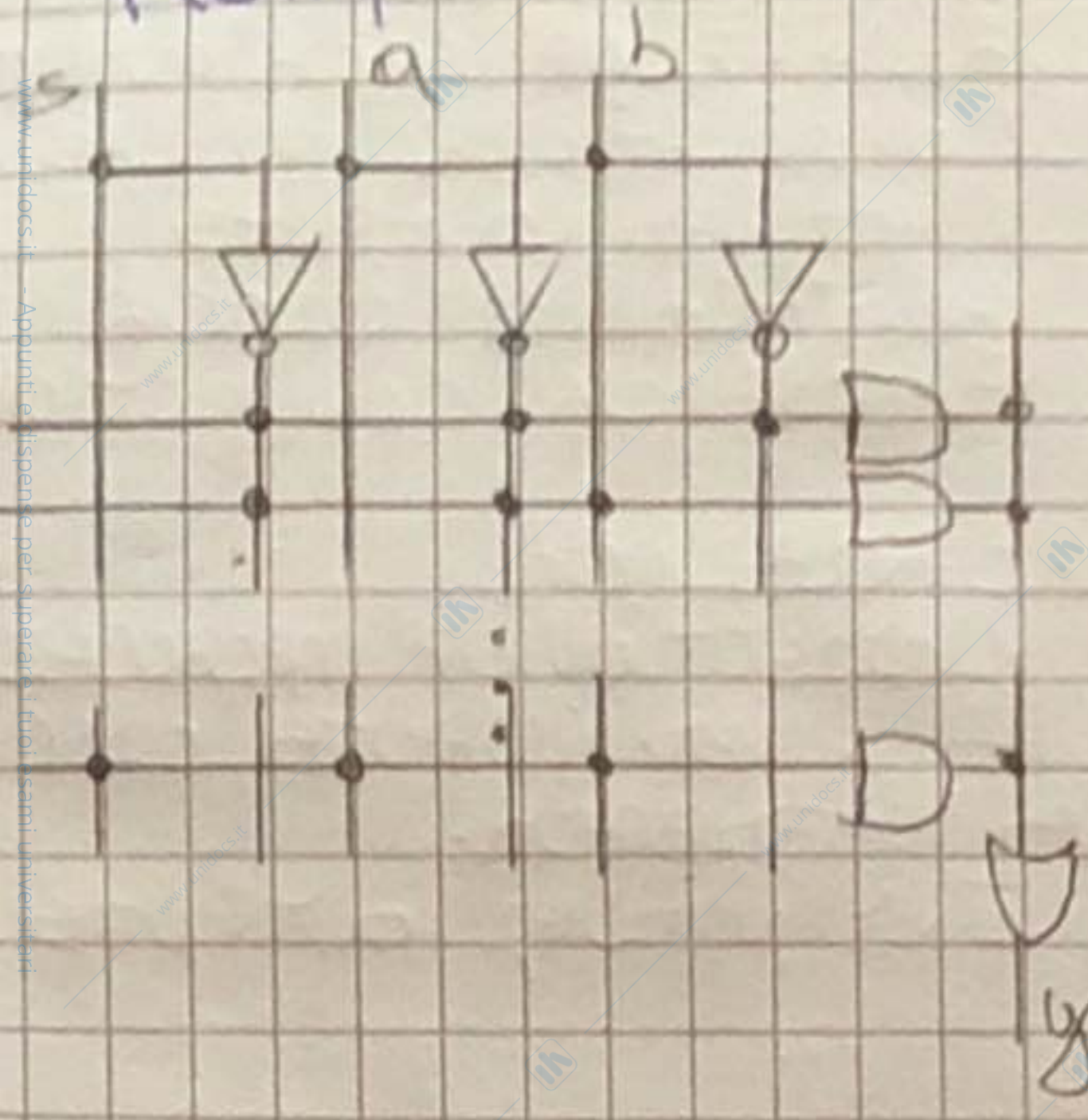
→ EXTENDED DATA O
PLEMENT SORT OF PI
HE NEXT COLUMN ADDRE
END.

→ SYNCHRONOUS DRA
OCATIONS SHOULD BE ACC
HE STARTING COLUMN
O OPERATE ON SUCCES
DGE OF THE CLOCK.

→ DOUBLE DATA RA
N MULTIPLE CLOCK EDG

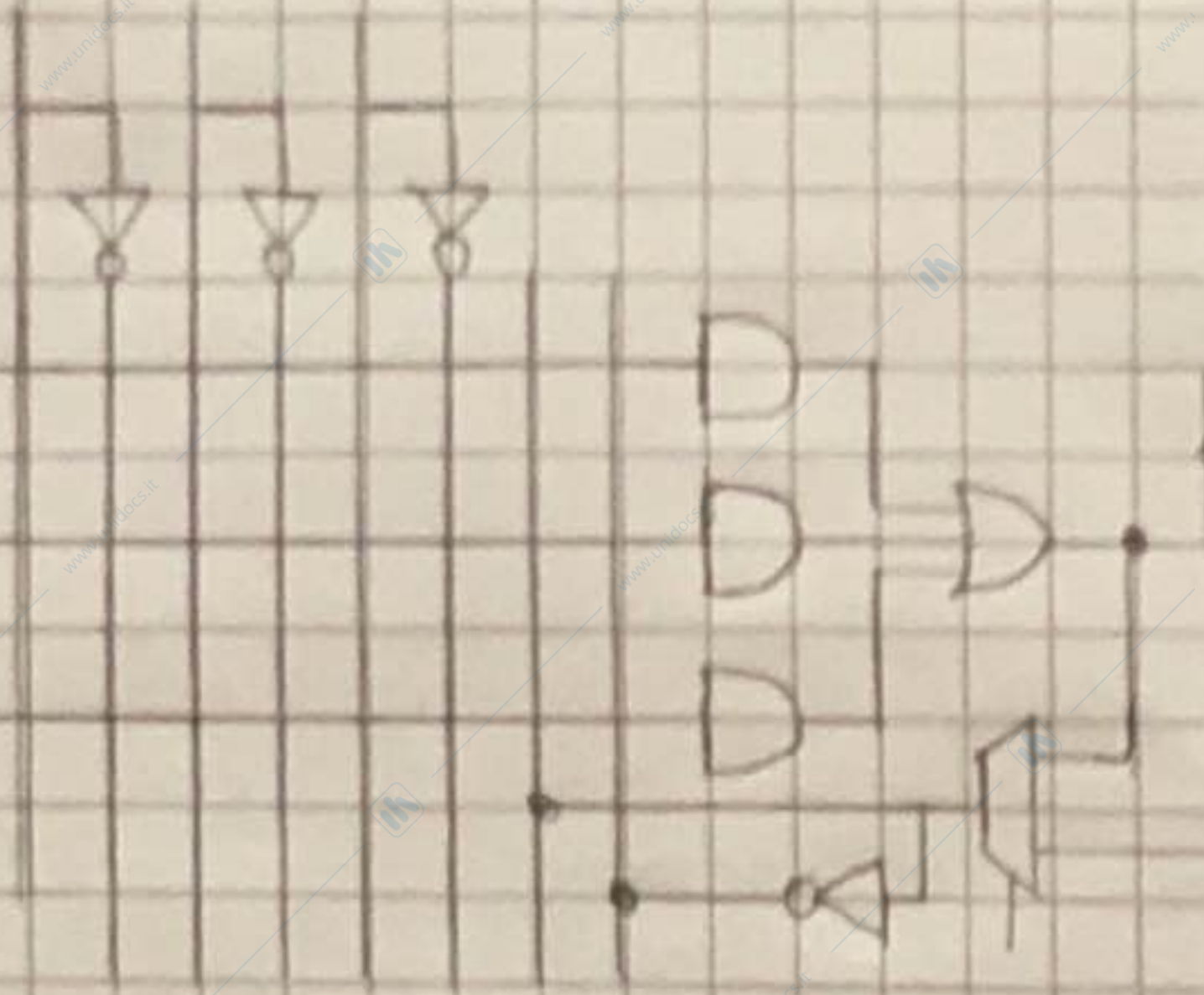
PROGRAMMABLE LOG

ROM



→ DISSAVANTAGES: MC
OF INPUTS.

MACRO CELLS (MC)

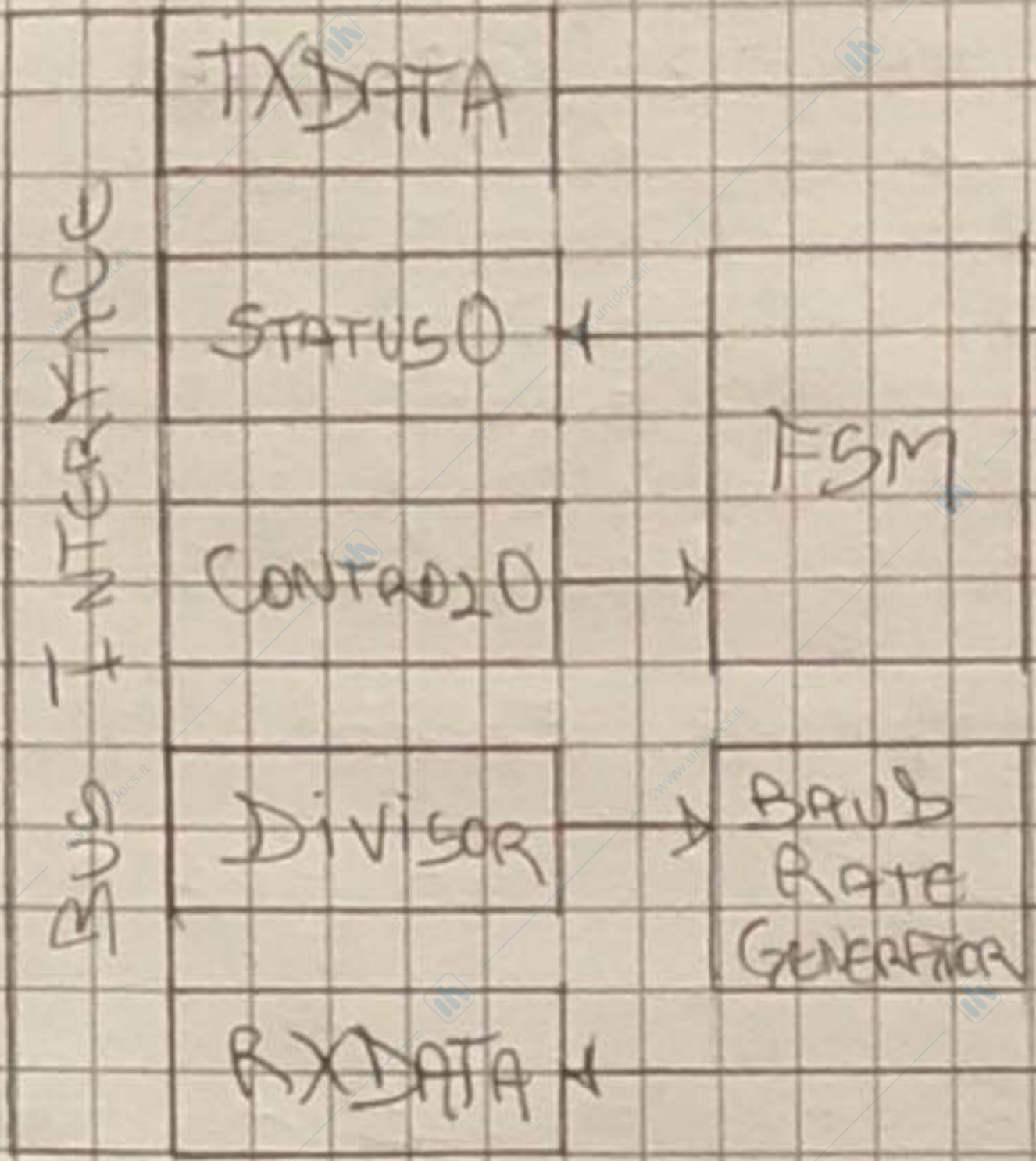


CP2D

→ COMPUTATION BLOCKS
MACROCELLS AND MACR
→ I/O BLOCK: CONFIG
EXTERNAL PINS (INPUT, O
PIN FEEDBACK)

INTERCONNECTIONS

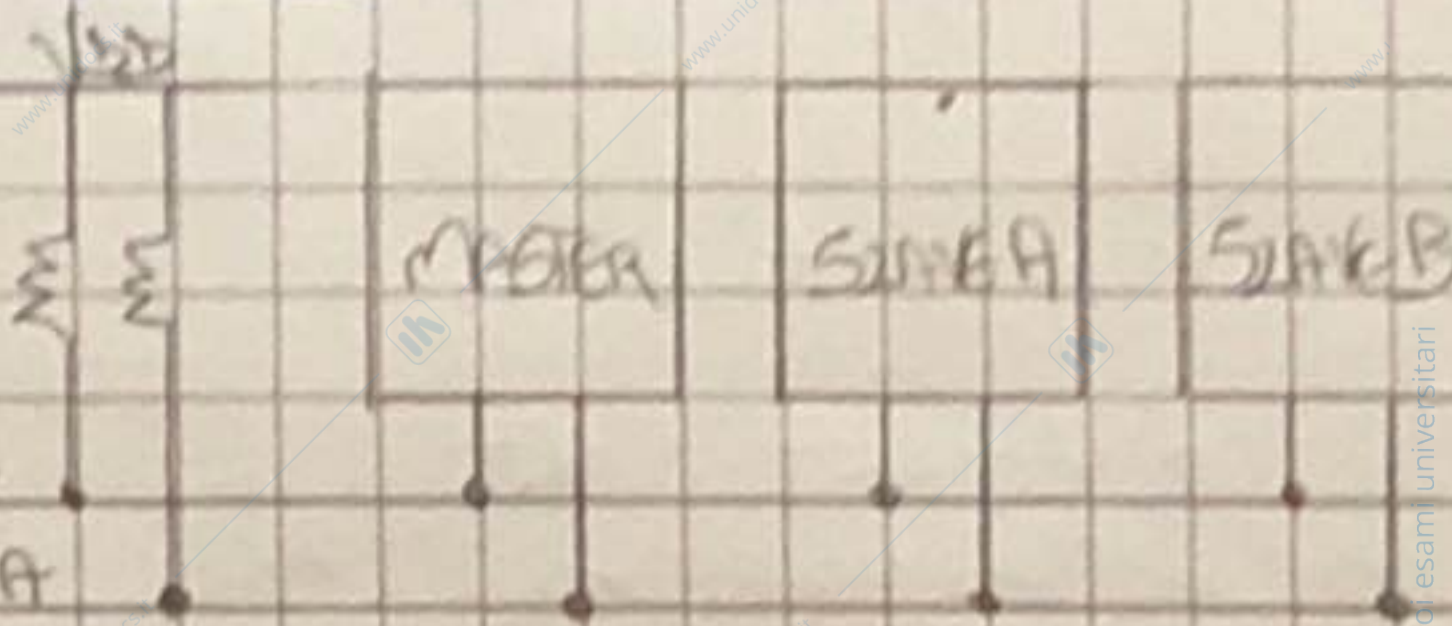
UART



BAUD RATE = NOMINAL

(UART (UNIVERSAL ...

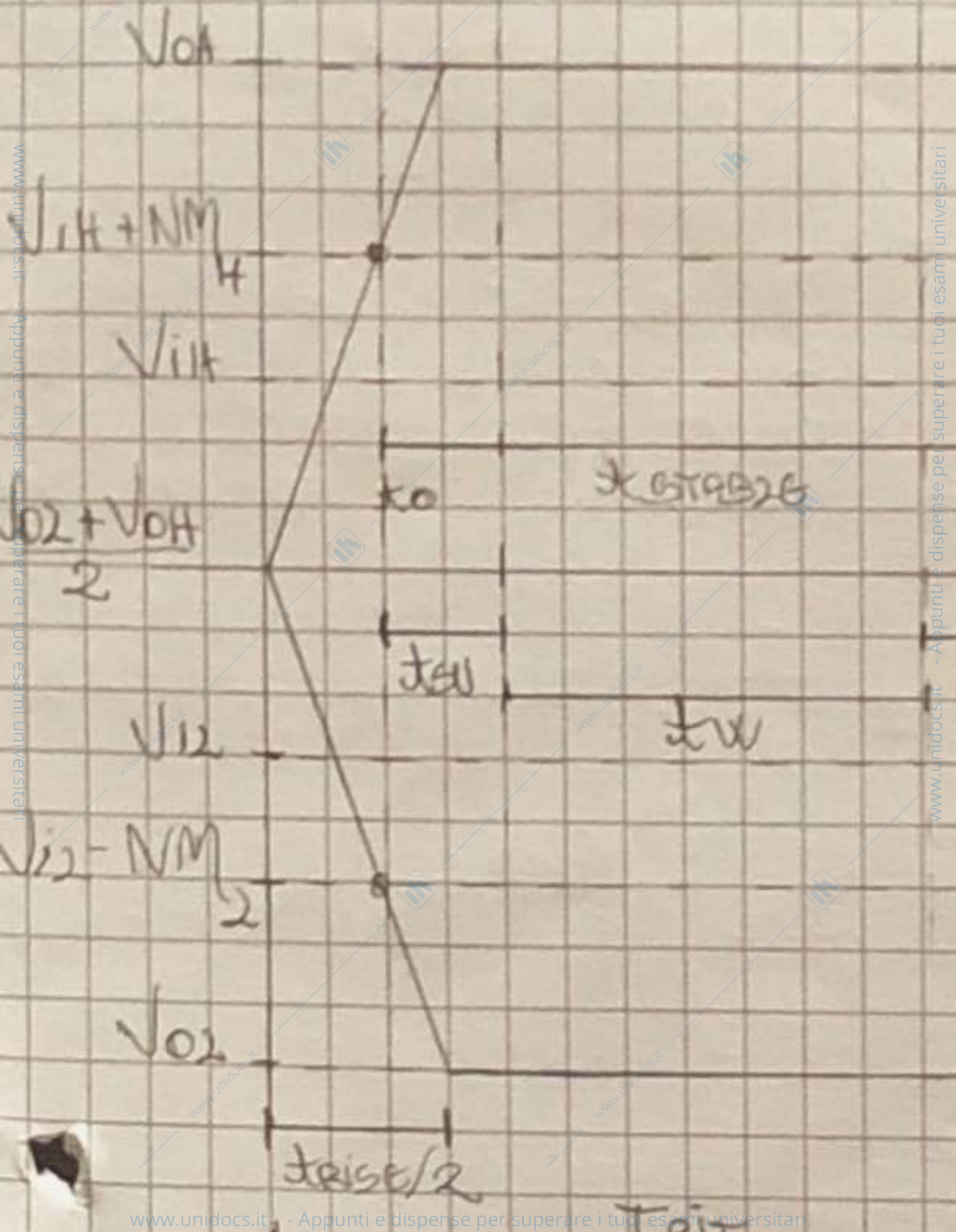
I2C



THE TARGET SLAVE ADDR
BIT FOLLOWS (R/$\overline{W}$), AN
• DATA: MASTER SEND
DATA AND ACK
• STOP: MASTER KEEP
THAT GOES HIGH, THEN B
• RESTART: MASTER
DOESN'T BECOME IDLE

→ CLOCK STRETCHIN
WHEN SDATA IS ALSO
ACTIVATES ITS OWN M
DRIVING LOGIC 0, SO IT

EYE DIAGRAM

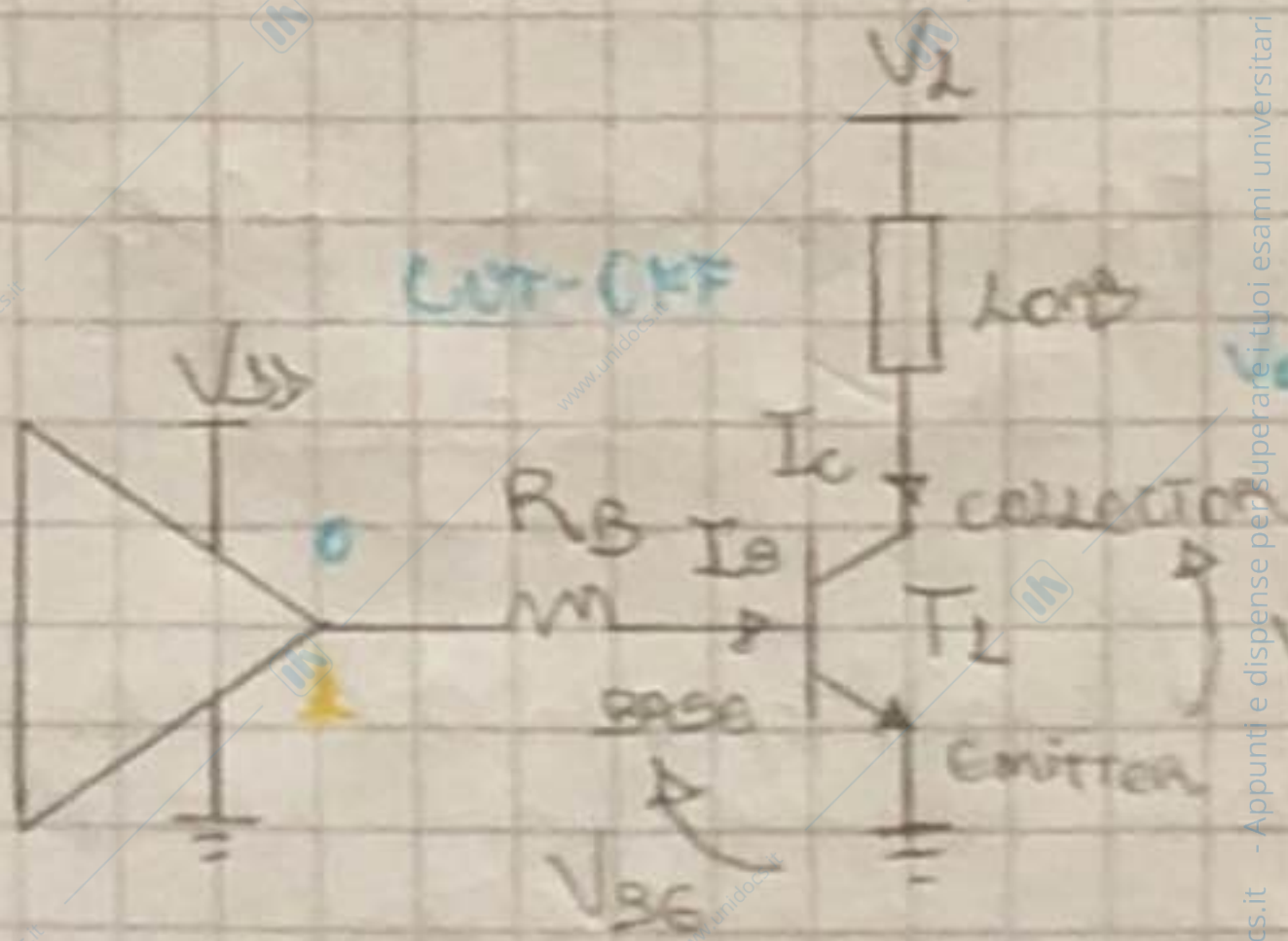


ENCODINGS

→ NON RETURN TO ZERO
ARE USED, AN BIT VALUE
WHEN A BIT VALUE CHA
VALUE KEEPS THE VOL
→ RETURN TO ZERO
ARE USED (UNIPOLAR)
THE OTHER BIT VALUES
LEVELS ARE USED (BI
TO A POSITIVE OR NEGA
→ MULTI LEVEL
LEVELS. THE BIT VA
THE BIT VALUE 1 INSE
DIRECTION DEPENDS ON
→ MANCHESTER: DA
PHASE MODULATION) TH
RECEIVED USES OF BIT
→ BIPHASE (BiΦ -
THE BEGINNING OF THE B
THE MIDDLE. LOGIC O

POWER MANAGEMENT

LOW SIDE npn BJT



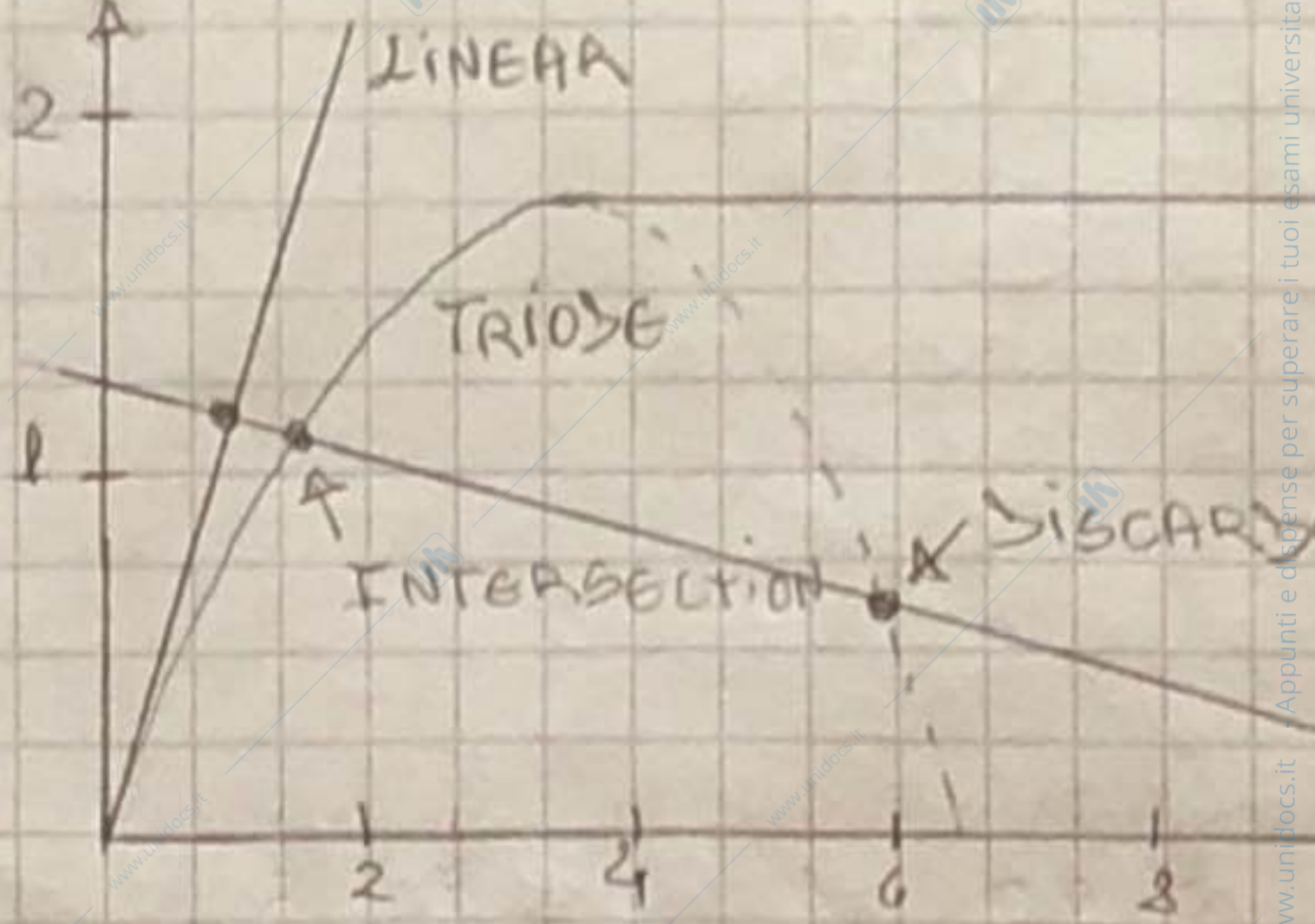
I_B SHOULD NOT EXCEED

$I_{BX} I_{CH} \Rightarrow \frac{V_{CH} - V_{BE}}{R_B}$

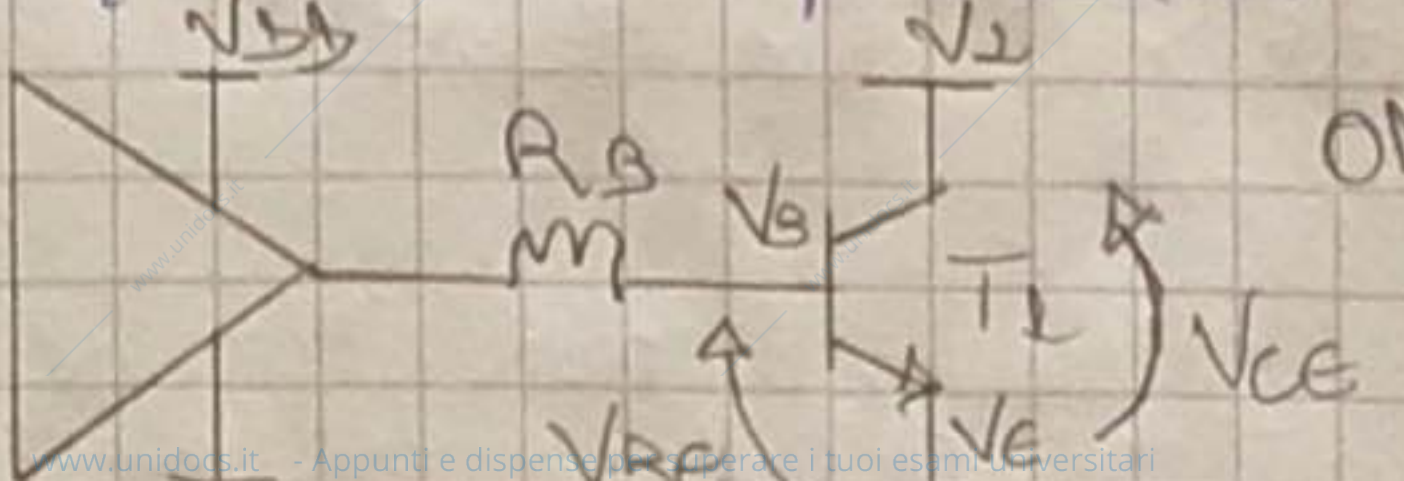
HIGHER R_B: LONGER

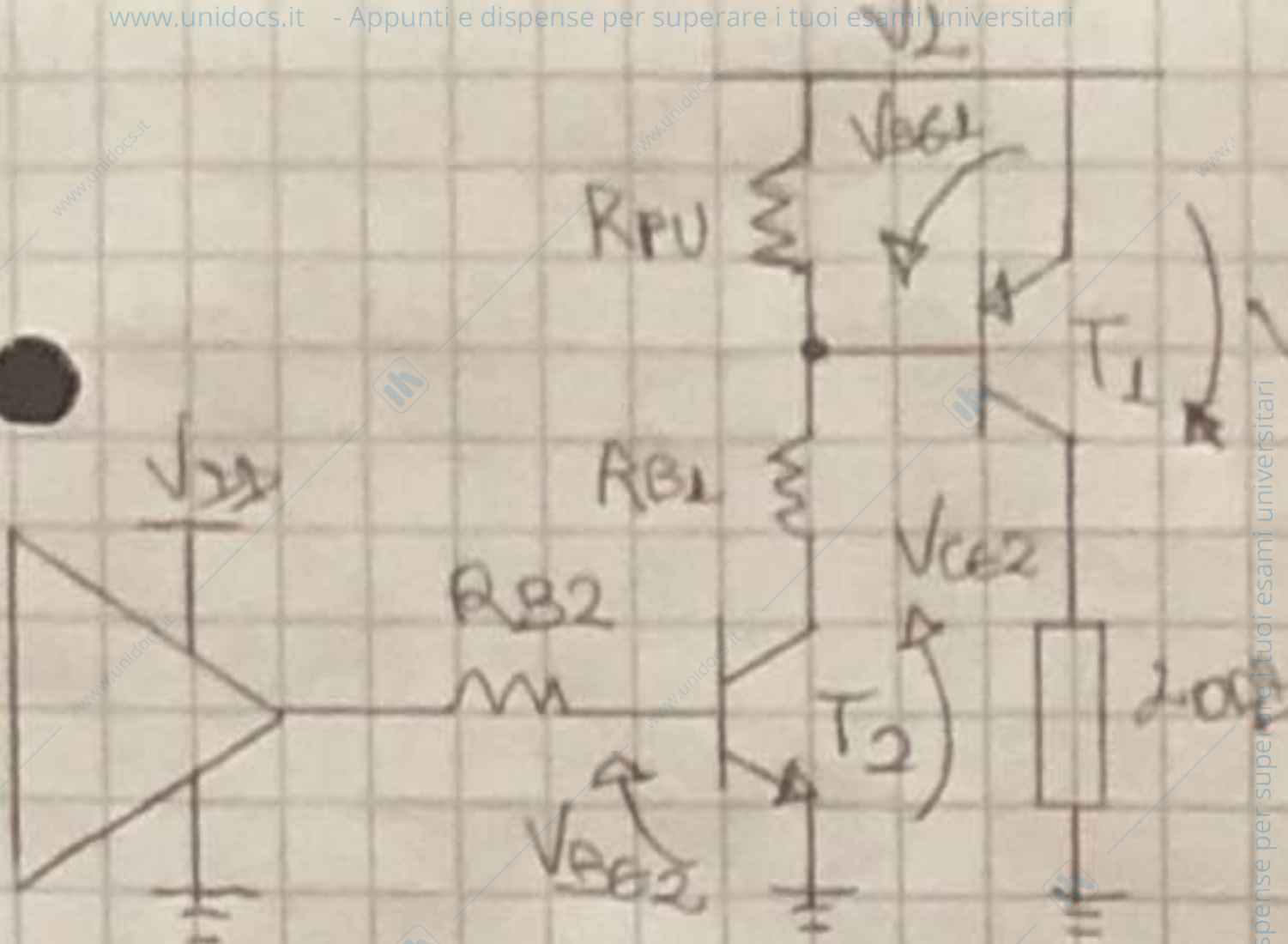
TRIODE REGION

$$I_{DS} = \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} \right]$$



HIGH SIDE mpm BJT





$$R_{B1} = \frac{V_{RB1}}{I_{B1}} \Rightarrow R_{B1}$$

COMPUTE NEEDED BASE

$$I_{B2} >> \frac{I_{C2}}{\beta_2}, \quad I_C$$

COMPUTE BASE R

$$\Delta I_L(t) = \frac{1}{L} V_L t = \frac{1}{L}$$

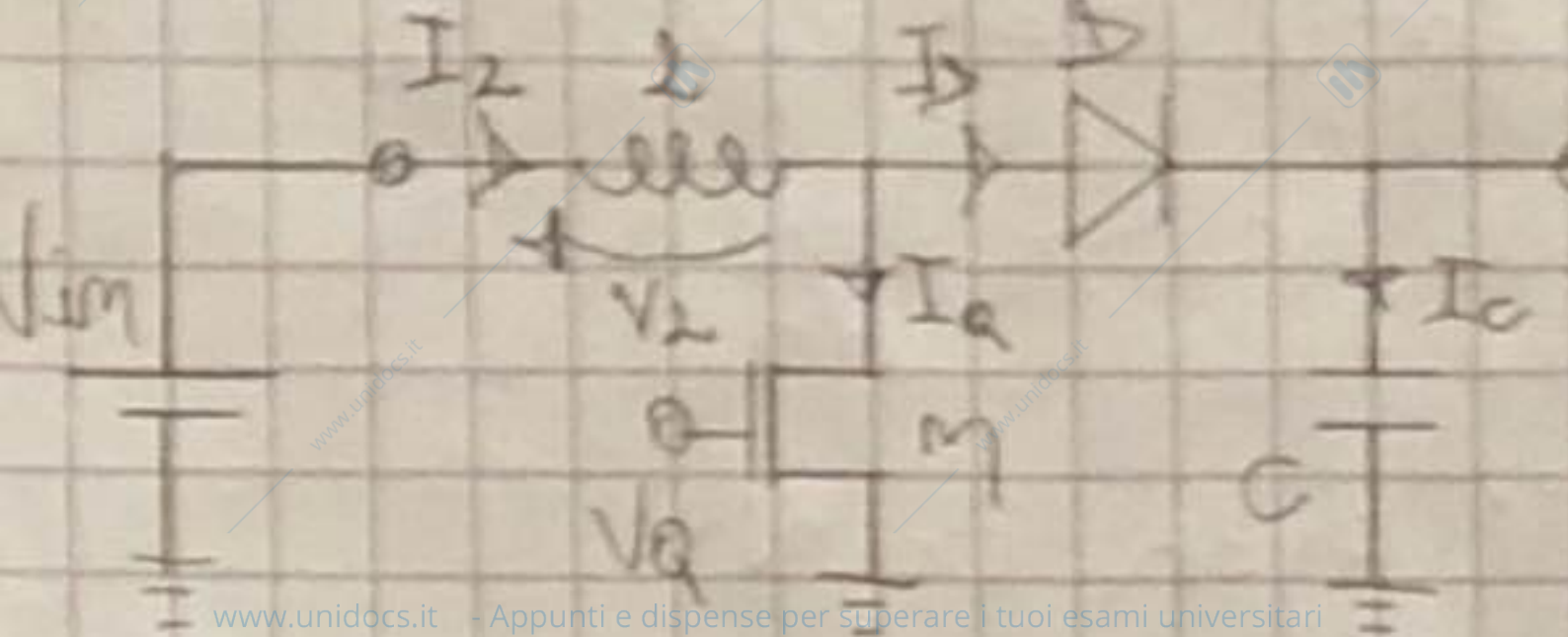
$$\Delta I_{L,OFF} = I_{L,M}$$

$$I_{L,max} = I_{out} + \frac{\Delta I_L}{2}$$

$$L > \frac{(1-\delta) V_{out}}{2 I_{out} f_{sw}} \quad , \quad I$$

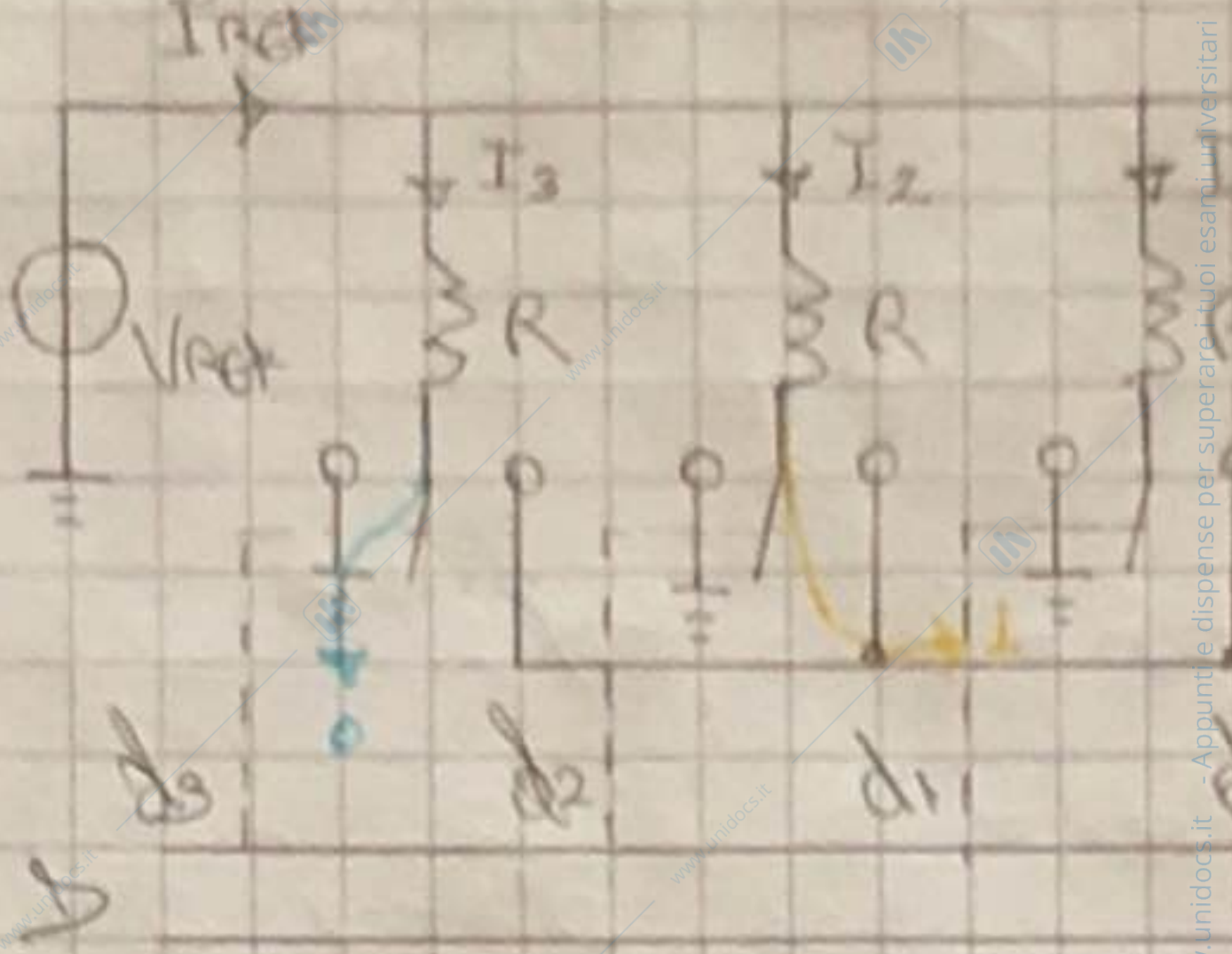
$$\Delta V_{out} = \frac{\Delta I_L}{8 C f_{sw}} \quad , \quad \Delta$$

Boost (Step Up)

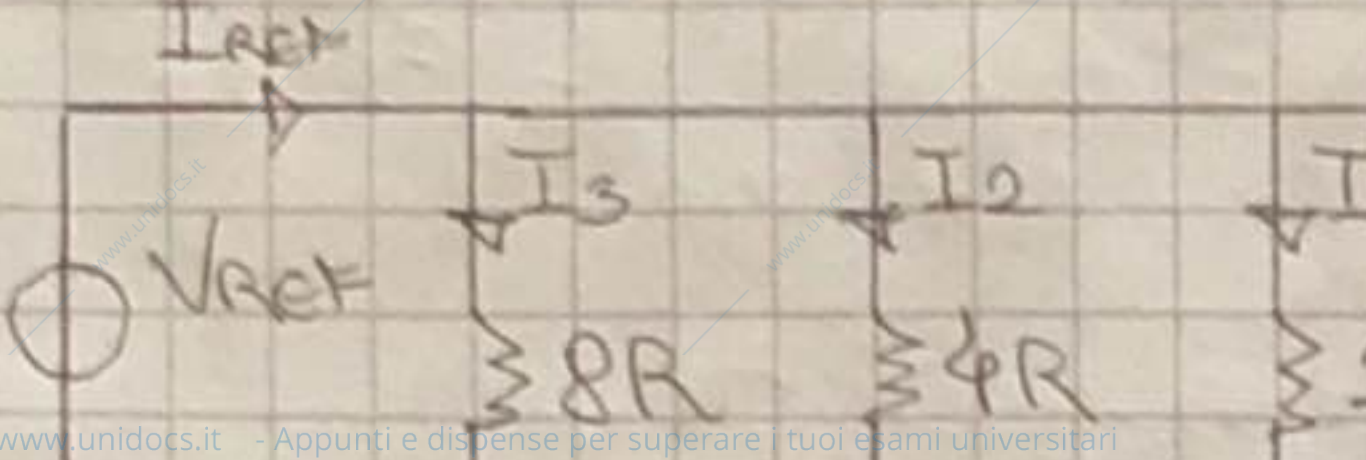


AD AND DA CONVER

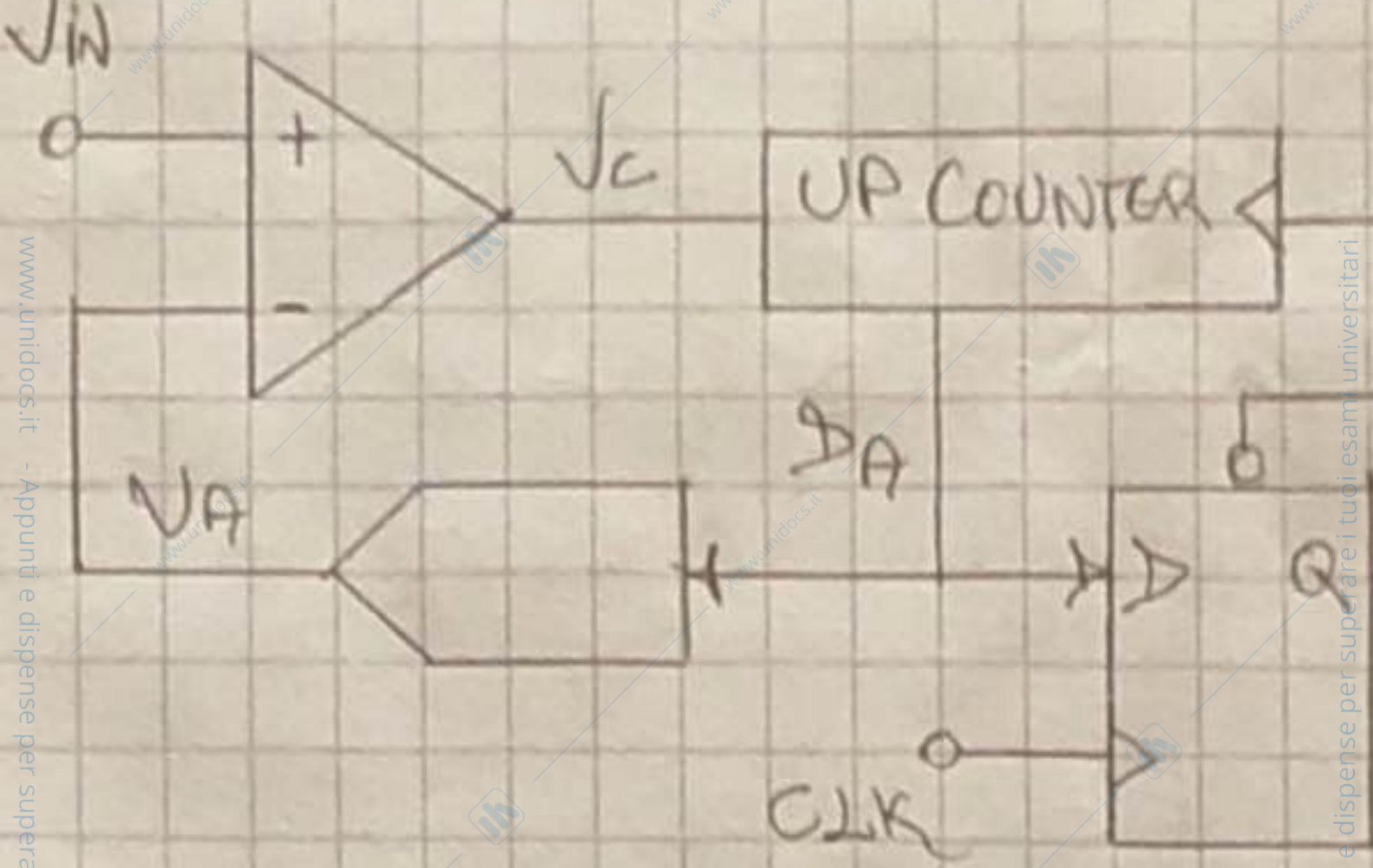
UNIFORM QUANTIZE



WEIGHTED QUANTIZ

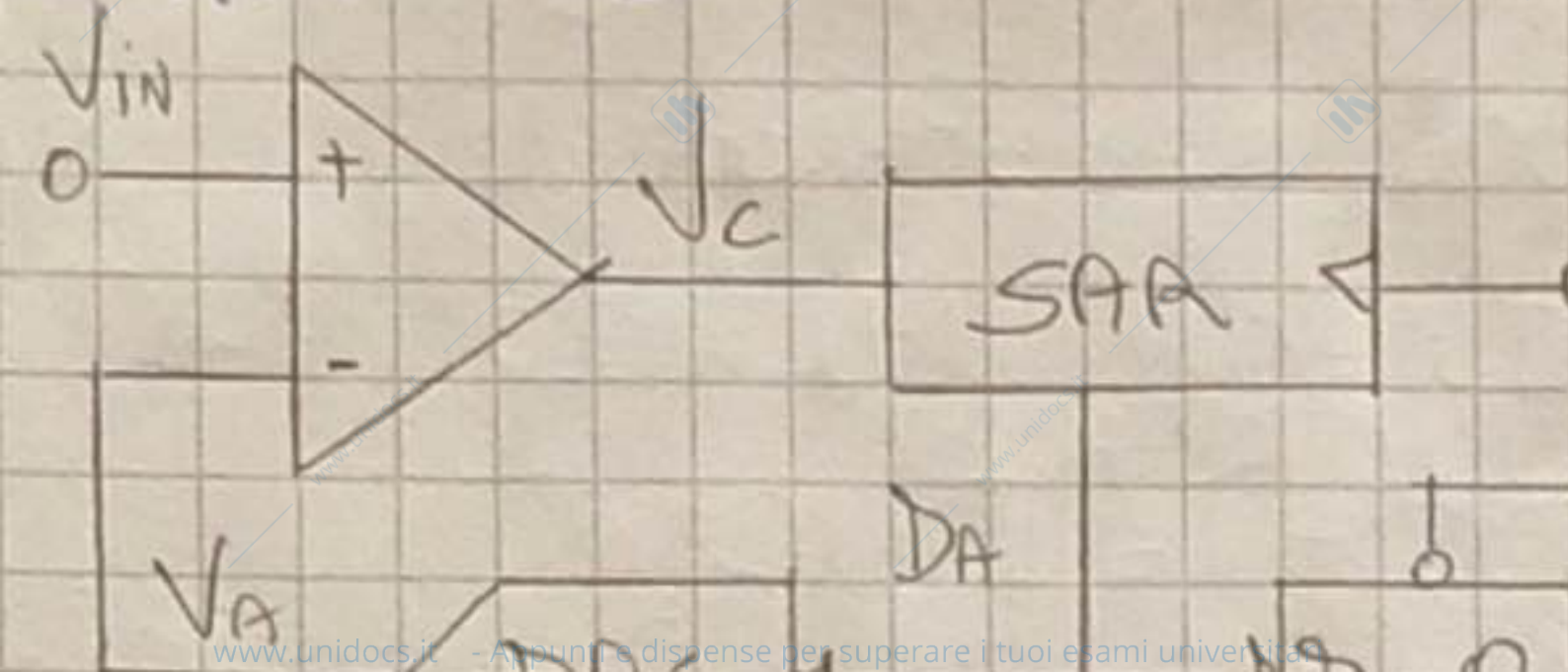


STAIRCASE ADC

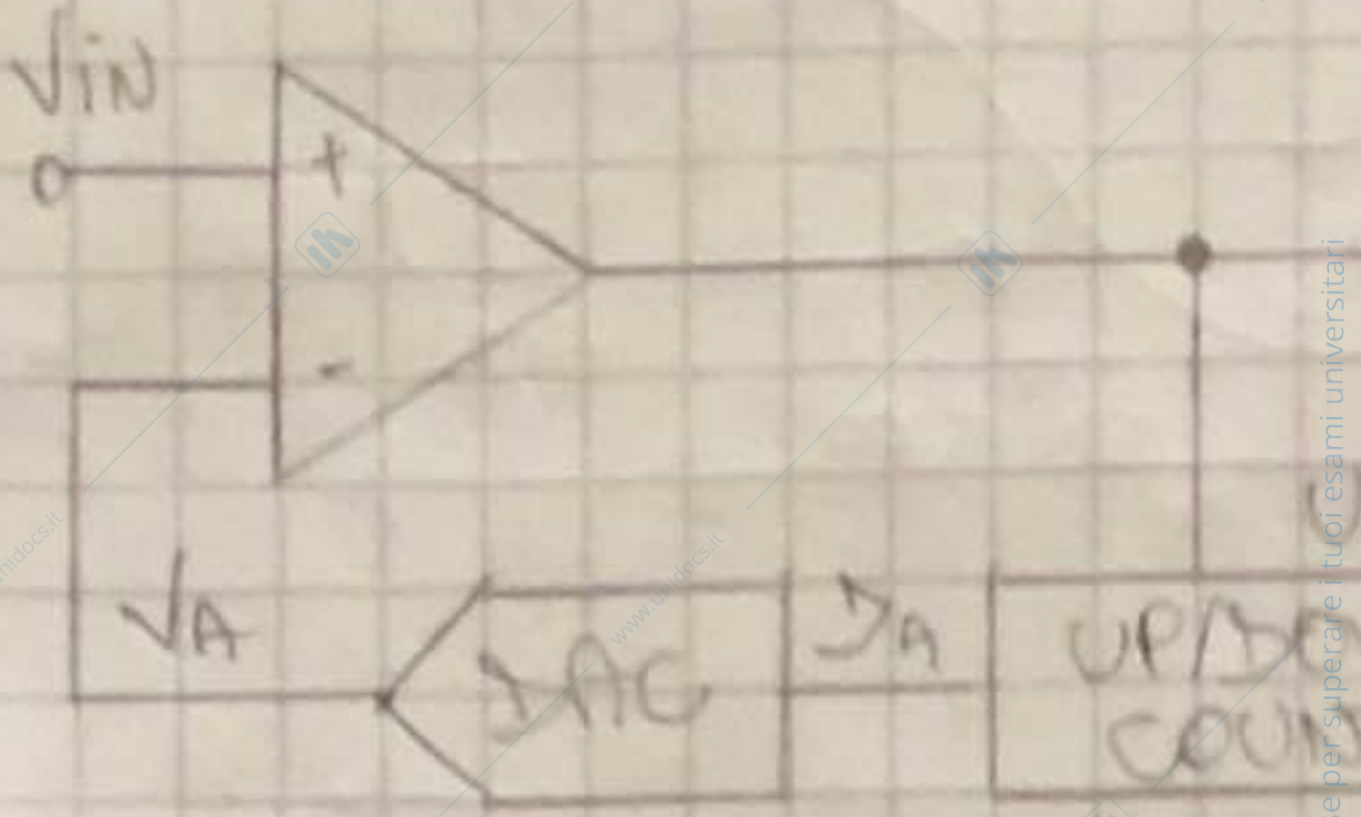


$$t_{CONV} = 2^{M_B} \cdot t_{CK}$$

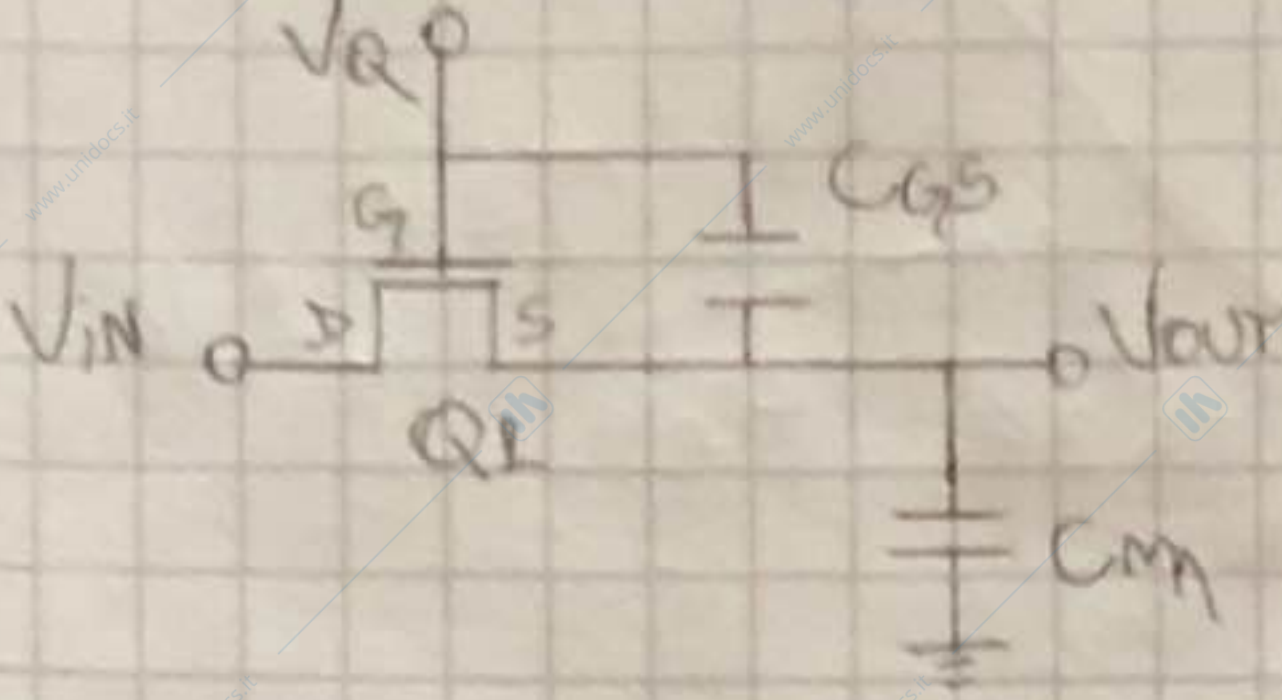
SAR ADC



DELTA (Δ) ADC



SAMPLE & HOLD ERROR



ACQUISITION TIME tacq

Sampling Time Jitter

After pedestal's trailing edge, second order deviations prevent the immediate of a conversion.

Jitter limits the maximum sampling frequency

Droop

Small leakage current during hold phase

$$\frac{dV_{out}}{dt} = \frac{I_{droop}}{C_m}, \quad \Delta V_{out}(t) = \frac{I_{droop}}{C_m}$$

Maximum voltage change

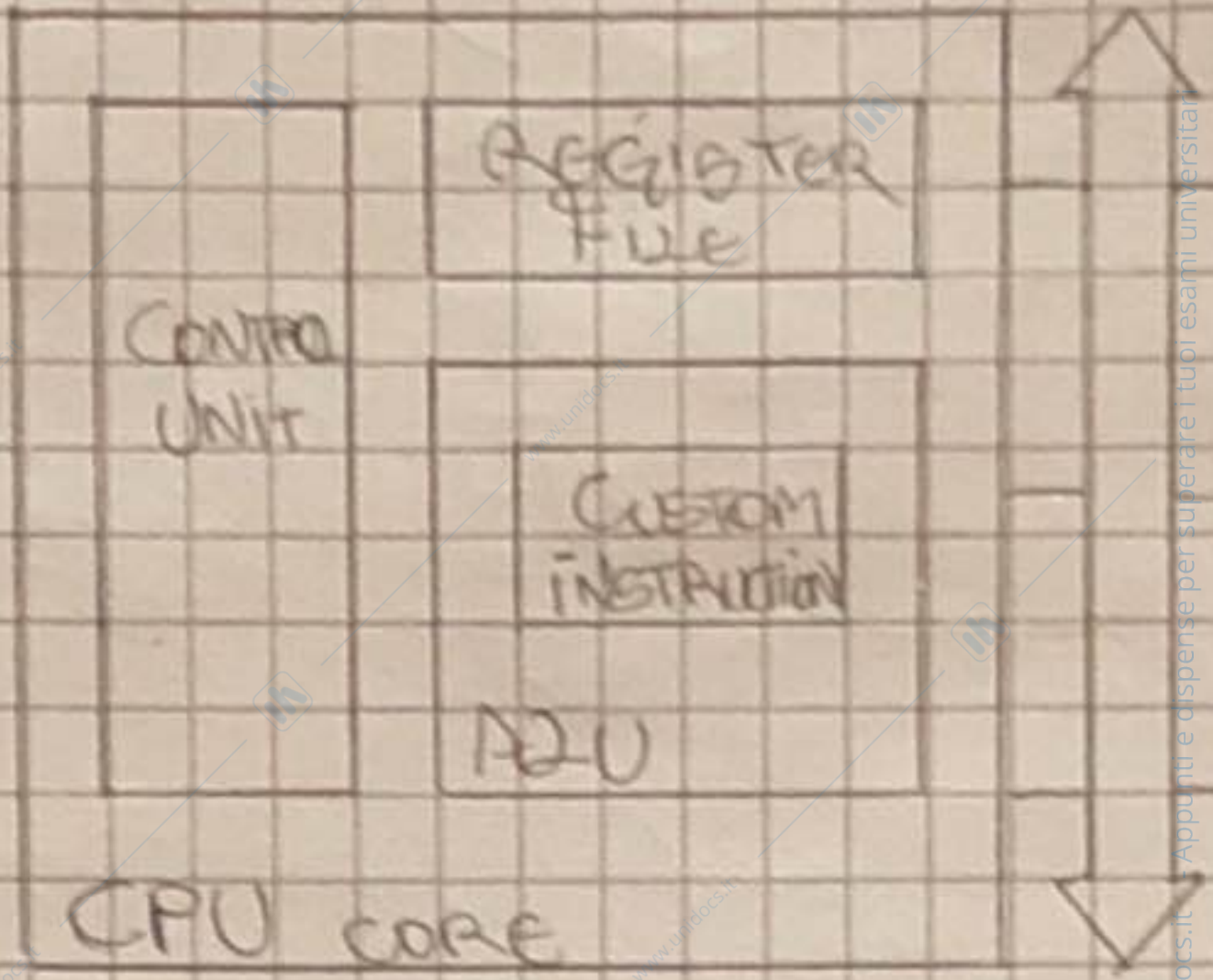
$$\Delta V_d = \frac{I_{droop}\, t_{conv}}{C_m}$$

Feedthrough

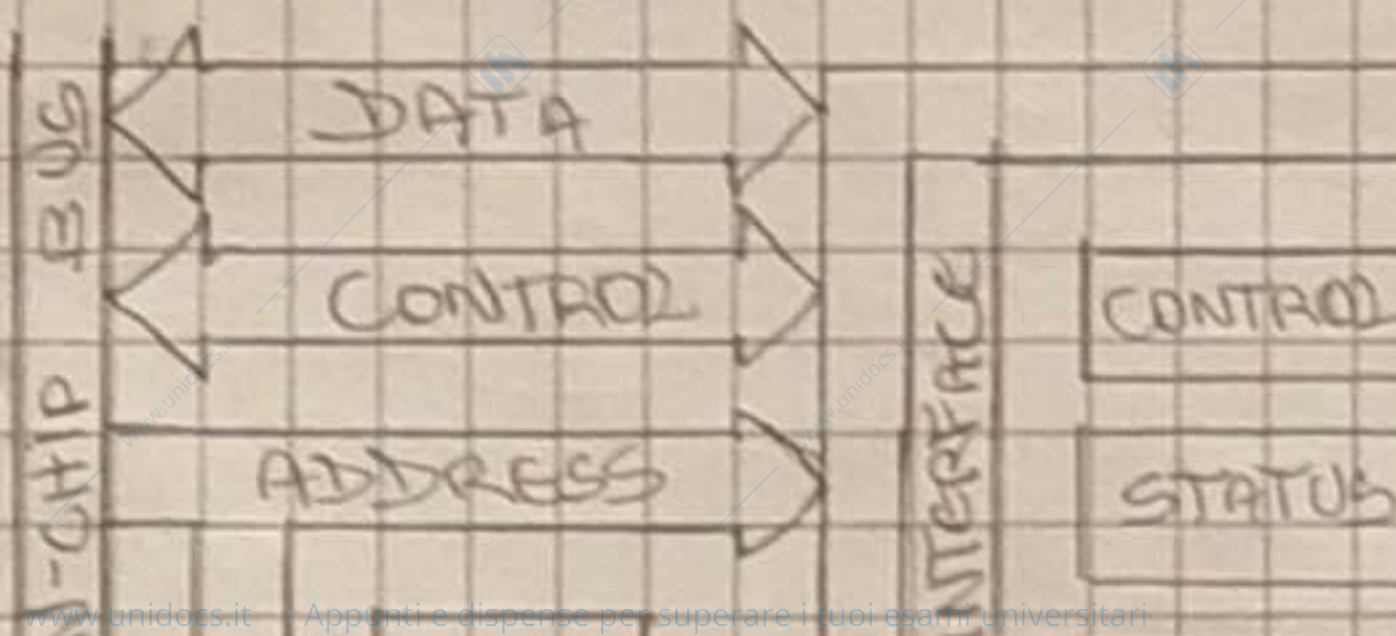
Changes on input signal induce a charge injection

PERIPHERALS

INTEGRATED CIRCUIT



PERIPHERALS



GPIO